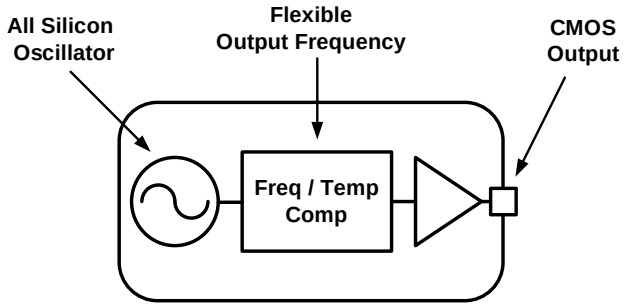
AS511 Arcadium™ Low Jitter CMOS Oscillator, 10 kHz to 125 MHz

The AS511 Arcadium™ all-silicon CMOS oscillator utilizes proprietary frequency synthesis and sensor technologies to provide a quartz-free, MEMS-free, low jitter clock at any output frequency. The device is factory-programmed to a fixed frequency ranging from 10 kHz to 125 MHz with < 0.026 ppb resolution and maintains low jitter across its operating range. It uses on-chip temperature and strain sensors, and an advanced LC tank architecture to achieve excellent reliabilities even in high impact shock scenarios.

AS511's on-chip power supply filtering provides industry-leading power supply noise rejection, simplifying the task of generating low jitter clocks in noisy systems that use switched-mode power supplies. Offered in an industry-standard packages of 2.5 x 3.2 mm, the AS511 has a dramatically simplified supply chain that enables Aeonsemi to ship samples shortly after receipt of order. Specific frequency and OE/ACT are factory programmed at time of shipment, eliminating the long lead times associated with custom frequencies. This process also guarantees 100% electrical testing of every device before shipment.



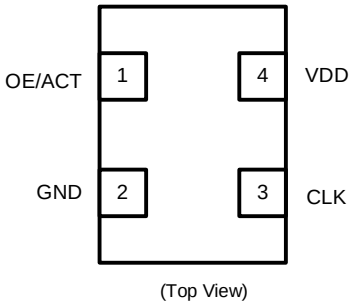
KEY FEATURES

- Quartz-free and MEMS-free without mechanical moving parts
- CMOS compatible output
- Available with frequencies from 10 kHz to 125 MHz
- Low jitter: 350 fs Typ RMS (12 kHz – 20 MHz bandwidth)
- 50 ppm stability (-40 to 85ºC)
- Integrated LDO for on-chip power supply noise filtering
- Support continuous 1.8V to 3.3V V_{DD} supply operation
- Industrial standard 2.5 x 3.2 mm package footprints

APPLICATIONS

- 1G/10G Ethernet
- Servers, switches, storage, NICs, search acceleration
- Test and measurement
- Clock and data recovery
- FPGA/ASIC clocking

Pin Assignments



(Top View)

2.5 x 3.2 mm

Pin #	Descriptions
1	OE = Output Enable. Active High ACT = Device Active. Active High
2	GND = Ground
3	CLK = Clock output
4	VDD = Power supply

1. Ordering Guide

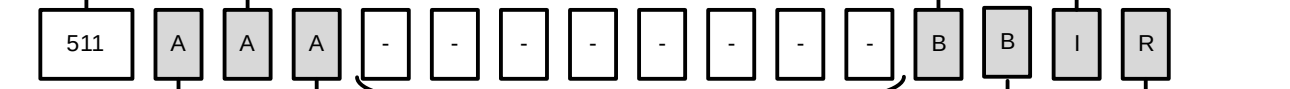
The AS511 Oscillator supports options including frequency and OE/ACT pin, as shown in the chart below. Specific device configurations are programmed into the part at time of shipment, and samples are available in 2 weeks.

XO Series	Description
511	CMOS Oscillator

	Total Stability [1]
A	± 50 ppm

	Package
B	2.5 x 3.2 mm

	Temperature Grade
I	-40 to 85 °C



	Freq Range
A	≤ 50 MHz
B	> 50 MHz

	Pin 1
A	OE
C	ACT

Device Revision

Frequency Code [2]	Description
Mxxxxxxx	F_{CLK} < 1 MHz
xMxxxxxx	1 MHz ≤ F_{CLK} < 10 MHz
xxMxxxxx	10 MHz ≤ F_{CLK} < 100 MHz
xxxMxxxx	100 MHz ≤ F_{CLK} ≤ 125 MHz

Tape and Reel	Package Qty
T	250
R	2500
<blank>	Sample

Notes:

1. Total stability includes temperature stability, initial accuracy, load pulling, V_{DD} variation, and 10 years aging at 40 °C.
2. For example: 125 MHz = 125M0000; 33.33333 MHz = 33M33333.

2. Electrical Specifications

Table 2.1. Electrical Specifications

V_{DD} = 1.8 V, 2.5 or 3.3 V ± 5%, T_A = –40 to 85 ºC

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Temperature Range	T_A		–40	—	85	ºC
Frequency Range	F_{CLK}	CMOS	0.01	—	125	MHz
Supply Voltage	V_{DD}		1.71		3.47	V
Supply Current (F_{CLK} = 50 MHz)	I_{DD}	Tristate Hi-Z (OE = 0, output disabled)	—	40	50	mA
		Ready State (ACT = 0, standby mode)	—	1	2	mA
		CMOS	—	40	55	mA
Total Stability[1]	F_{STAB}	Frequency stability	–50	—	50	ppm
Rise/Fall Time (20% to 80% V_{PP})	T_R/T_F	CMOS (C_L = 5 pF)	—	0.5	1.5	ns
Duty Cycle	D_C	All formats	45	—	55	%
Output Enable (OE)[2]	V_{IH}		0.7 × V_{DD}	—	—	V
	V_{IL}		—	—	0.3 × V_{DD}	V
	T_D	Output Disable Time, F_{CLK} >10 MHz	—	—	3	µs
	T_E	Output Enable Time, F_{CLK} >10 MHz	—	—	20	µs
Powerup Time	t_{OSC}	Time from 0.9 × V_{DD} until output frequency (F_{CLK}) within spec	—	—	4	ms
CMOS Output	V_{OH}	I_{OH} = 8/6/4 mA for 3.3/2.5/1.8V V_{DD}	0.83 × V_{DD}	—	—	V
	V_{OL}	I_{OL} = 8/6/4 mA for 3.3/2.5/1.8V V_{DD}	—	—	0.17 × V_{DD}	V

Notes:

1. Total Stability includes temperature stability, initial accuracy, load pulling, V_{DD} variation, and aging for 10 years at 40ºC.
2. OE/ACT includes a 50 kΩ pull-up to VDD for OE/ACT active high. Includes a 50 kΩ pull-down to GND for OE/ACT active low.

Table 2.2. Clock Output Phase Jitter and PSRR

V_{DD} = 1.8 V, 2.5 or 3.3 V ± 5%, T_A = –40 to 85 ºC

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Phase Jitter (RMS, 12 kHz - 20 MHz)[1,2] F_{CLK} ≥ 10 MHz	ϕ_J	CMOS	—	350	—	fs
Spurs Induced by External Power Supply Noise, 50 mVpp Ripple. CMOS 125 MHz Output V_{DD} = 1.8 V	PSRR	100 kHz sine wave	—	-76	—	dBc
		200 kHz sine wave	—	-75	—	
		500 kHz sine wave	—	-75	—	
		1 MHz sine wave	—	-75	—	
Spurs Induced by External Power Supply Noise, 50 mVpp Ripple. CMOS 125 MHz Output V_{DD} = 2.5 or 3.3 V	PSRR	100 kHz sine wave	—	-83	—	dBc
		200 kHz sine wave	—	-83	—	
		500 kHz sine wave	—	-83	—	
		1 MHz sine wave	—	-82	—	

Note:

1. Applies to output frequency: 50, 100, 125 MHz.
2. Guaranteed by characterization. Jitter inclusive of any spurs.

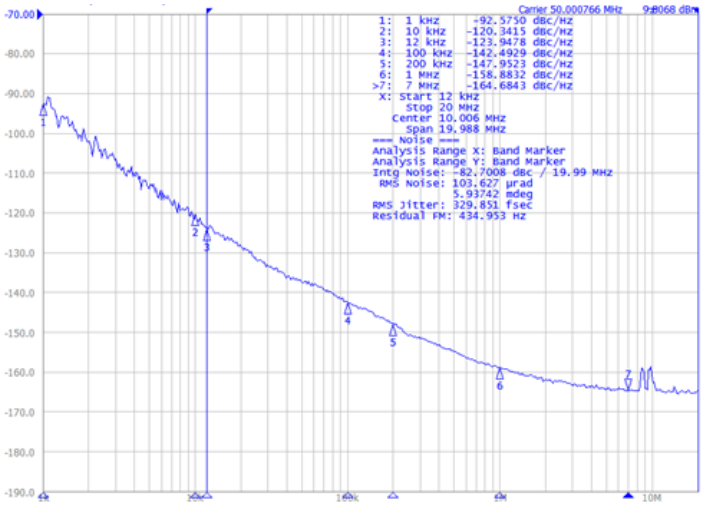


Figure 2.1: Phase Noise at 50 MHz

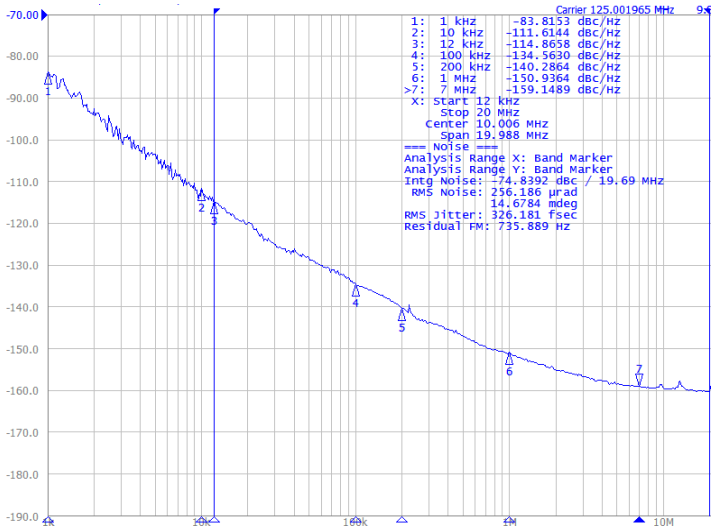


Figure 2.2: Phase Noise at 125 MHz

Table 2.3. Environmental Compliance and Package Information

Parameter	Test Condition
Moisture Sensitivity Level	1

Note:

For additional product information not listed in the data sheet (e.g. RoHS Certifications, MSDS data, qualification data, REACH Declarations, ECCN codes, etc.), contact aeonsemi.com/contact-us/

Table 2.4. Thermal Conditions

Package	Parameter	Symbol	Test Condition	Value	Unit
2.5 x 3.2 mm, 4-pin DFN	Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air	108	ºC/W
	Thermal Resistance Junction to Board	Θ_{JB}	Still Air	84	ºC/W
	Max Junction Temperature	T_J	Still Air	125	ºC

Table 2.5. Absolute Maximum Ratings[1]

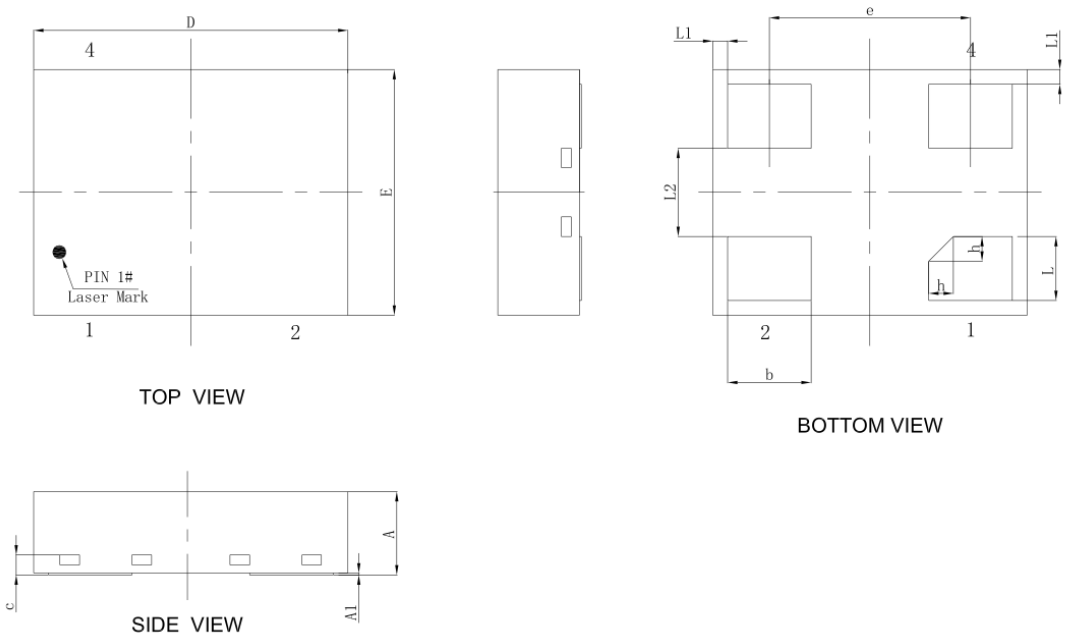
Parameter	Symbol	Rating	Unit
Maximum Operating Temperature[2]	T_{AMAX}	85	ºC
Storage Temperature	T_S	-55 to 125	ºC
Supply Voltage	V_{DD}	-0.5 to 3.8	V
Input Voltage	V_{IN}	-0.5 to V_{DD} + 0.3	V
ESD HBM (JESD22-A114)	HBM	4.0	kV
Solder Temperature[2]	T_{PEAK}	260	ºC
Solder Time at T_{PEAK}[2]	T_P	20 - 40	sec

Notes:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

3. Package Outline

The figure below illustrates the package details for the AS511. The table below lists the values for the dimensions shown in the illustration.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.80	0.85	0.90
c	0.203REF		
D	3.10	3.20	3.30
e	2.05BSC		
E	2.40	2.50	2.60
L	0.60	0.65	0.70
L1	0.10	0.15	0.20
L2	0.85	0.90	0.95
h	0.20	0.25	0.30

Figure 5.1. AS511 (2.5 x 3.2 mm) Outline Diagram

4. PCB Land Pattern

The figure below illustrates the PCB land pattern for the AS511. The table below lists the values for the dimensions shown in the illustration.

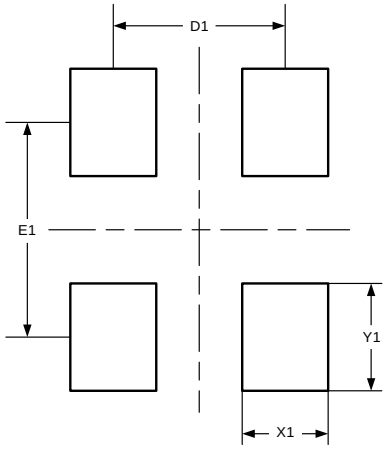


Figure 4.1. AS511 PCB Land Pattern

Table 4.1. PCB Land Pattern Dimensions (mm)

Dimension	Description	2.5 x 3.2 mm Package Value (mm)
X1	Width - leads on long sides	0.65
Y1	Height - leads on long sides	0.85
D1	Pitch in X directions of XLY1 leads	1.55
E1	Lead pitch XLY1 leads	2.05

Notes: The following notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 0.8:1 for the pads.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

5. Top Marking

The figure below illustrates the mark specification for the AS511. The table below lists the line information.

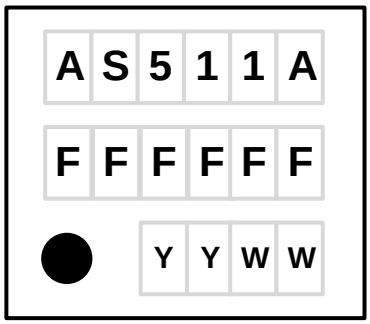


Figure 5.1. AS511 Top Mark

Table 5.1. AS511 Top Mark Description

Line	Position	Description
1	1–6	AS511 = Device name; A = "≤ 50 MHz"; B = "> 50 MHz"
2	**Trace Code**	
	1–6	6 digits trace code per assembly release instructions
3	Position 1	Pin 1 orientation mark (dot)
	Position 2–3	Year (last two digits of the year), to be assigned by assembly site (ex: 2017 = 17)
	Position 4–5	Calendar Work Week number (1–53), to be assigned by assembly site

6. Revision History

Revision 0.0

Feb 2021

- Initial release