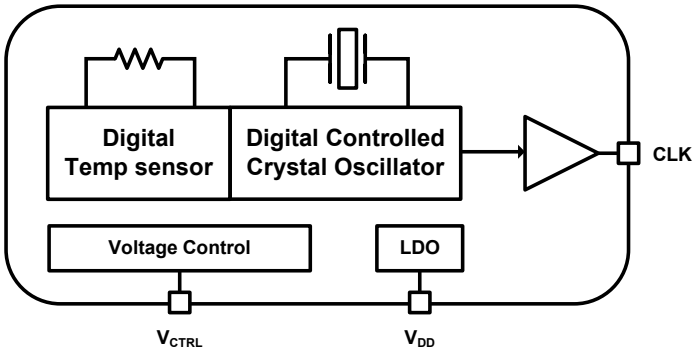
AS5234 Ultra Low Jitter Low Power LVCMOS VCTCXO

Description

The AS5234 is a voltage-controlled temperature-compensated crystal oscillator (VCTCXO) that provides a low-amplitude 0.8 V LVCMOS output from 10 MHz to 76.8 MHz. Digital temperature sensing and frequency compensation maintain a stable reference clock, while the voltage-control input enables smooth frequency adjustment around the factory-programmed nominal frequency.

The tuning slope is programmable for the required application, with a maximum slope of 6 ppm/V. The center control voltage and frequency pull range are factory configured through the device ordering code. An integrated LDO provides robust power supply noise rejection and simplifies external supply filtering over the 1.8 V to 3.3 V operating range.

The AS5234 is available in the standard 2016 package with industrial, extended industrial, and automotive temperature grades. Its wide operating range, low-jitter output, and programmable voltage control support precision timing in GNSS receivers, communication equipment, storage platforms, servers, and test and measurement instruments.



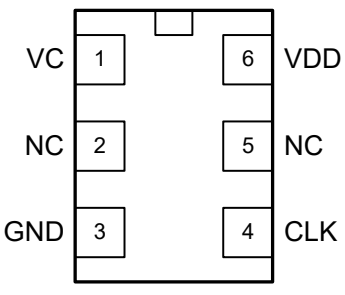
Key Features

- Frequency range: 10 to 76.8 MHz
- 0.8 V LVCMOS output
- Ultra-low jitter: 93 fs Typ RMS
  (12 kHz – 20 MHz, @76.8 MHz)
- Operating temperature range:
  - -40 to 85 ℃ (Industial grade)
  - -40 to 105 ℃ (Extended-Industial grade)
  - -40 to 105 ℃ (AEC-Q100 grade 2)
- Temperature stability:
  - ±0.5 ppm (Grade C)
  - ±20 ppm (Grade D)
- Programmable tuning slope up to 6 ppm/V
- Integrated LDO for on-chip power supply noise filtering
- Support 1.8V, 2.5V, 3.3V V_{DD} supply operation
- Standard DFN 2016 package

Application

- Precision GNSS systems
- Microwave backhaul
- Narrow-band communications
- Storage and servers
- Test and measurements

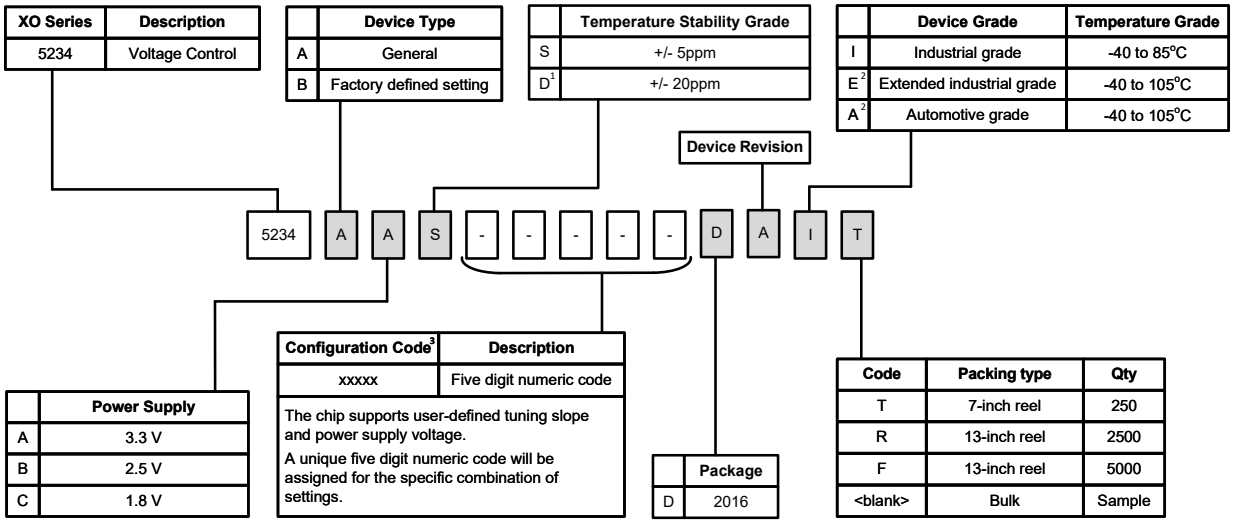
Pin definition



Top view

Pin#	Description
1	VC = Voltage control input
2	NC = Not connect
3	GND = Ground
4	CLK = Clock output
5	NC = Not connect
6	VDD = Power supply

1. Ordering Guide



Note:

1. Temperature compensation is not applied for grade-D device. Frequency is calibrated at 25 ℃ in production test.
2. Contact Aeonsemi for extended-industrial and automotive-grade devices.
3. The five-digit numeric code is an identification of the configurations. Check the datasheet appendix for the details.

2. Electrical Specifications

Table 2.1. Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
Operating Temperature Range						
Temperature Range	T_A	-40	–	85	℃	Industrial grade
		-40	–	105	℃	Extended industrial grade
		-40	–	105	℃	Automotive AEC-Q100 Grade2
Supply Voltage and Power Consumption						
Supply Voltage	V_{DD}	1.62	–	3.63	V	Core voltage
Driver Regulator Voltage	V_R	0.8	–	1.2	V	Regulator voltage
Supply Current	I_{CORE}	–	4	5	mA	Tristate Hi-Z (Output disabled)
(F_{CLK} = 38.4 MHz)	I_{DRV}	–	1.6	2	mA	0.8V LVCMOS (Load=10pF//10kΩ)
Frequency Range						
Frequency Range	F_{CLK}	10	–	76.8	MHz	Standard frequency options
		10, 16, 19.2, 20, 25, 26, 32, 38.4, 50, 52				Contact Aeonsemi for other frequency options
Frequency Tolerance						
Initial frequency accuracy[1]	F_{INIT}	-2	–	2	ppm	Grade C
		-5	–	5	ppm	Grade D
Temperature stability over full temp range[2]	F_{STAB}	-0.5	–	0.5	ppm	Grade C
		-20	–	20	ppm	Grade D
Aging	S_{AGING}	-1	–	1	ppm/y	Maximum aging slope at 25 ℃
	F_{AGING}	-3	–	3	ppm	10-year aging at 25℃
Notes: 1. Inclusive of initial frequency tolerance at 25℃, variations over supply voltage, load and humidity after 2 times of reflows. 2. Frequency / temperature characteristics with offset removed.						
VCXO Control Characteristics						
Control voltage input	V_C	0	–	V_{DD}	V	Input reference voltage range
Center control voltage[3]	V_{CEN}	–	$V_{DD}/2$	–	V	Factory-programmable center voltage
Tuning slope[3]	K_V	–	–	6	ppm/V	Factory-programmable tuning slope
Control voltage linearity	Lin	-3	–	3	%	Linearity error
Notes: 3. The center control voltage and tuning slope are factory-programmable to meet application-specific requirements. Contact aeonsemi.com/contact_us to obtain the unique part number for the required configuration.						
Output Characteristics						
Powerup time	T_{OSC}	–	–	4	ms	Time from power reaches 0.9 × V_{DD} to output frequency (F_{CLK}) within spec
Duty cycle	DC	45	–	55	%	0.8V LVCMOS (Load=10pF//10kΩ)
Rise/Fall time (20% to 80% VPP)	$T_{R/F}$	–	0.5	1.5	ns	0.8V LVCMOS (Load=10pF//10kΩ)
Output amplitude	V_O	–	0.8	–	V_{PP}	LVCMOS output

Continued on next page

Parameter	Symbol	Min	Typ	Max	Unit	Note
Phase Noise and Jitter						
RMS jitter	R_J	–	100	200	fs	F_{CLK} >= 50 MHz
BW: 12k - 20MHz		–	150	300	fs	F_{CLK} <50 MHz
Phase noise	PN_{10}	–	-89	–	dBc/Hz	Phase noise at 10Hz offset
38.4MHz LVCMOS output	PN_{100}	–	-119	–	dBc/Hz	Phase noise at 100Hz offset
V_{DD} = 1.8 - 3.3V	PN_{1k}	–	-143	–	dBc/Hz	Phase noise at 1kHz offset
	PN_{10k}	–	-152	–	dBc/Hz	Phase noise at 10kHz offset
	PN_{100k}	–	-158	–	dBc/Hz	Phase noise at 100kHz offset
	PN_{1M}	–	-162	–	dBc/Hz	Phase noise at 1MHz offset
	PN_{10M}	–	-163	–	dBc/Hz	Phase noise at 10MHz offset
PSNR						
Spurs from power noise	PSNR	–	-76	–	dBc	100 kHz sine wave
50mV ripple		–	-75	–	dBc	200 kHz sine wave
V_{DD} = 1.8V		–	-75	–	dBc	500 kHz sine wave
		–	-75	–	dBc	1 MHz sine wave
Spurs from power noise	PSNR	–	-83	–	dBc	100 kHz sine wave
50mV ripple		–	-83	–	dBc	200 kHz sine wave
V_{DD} = 2.5 or 3.3V		–	-83	–	dBc	500 kHz sine wave
		–	-82	–	dBc	1 MHz sine wave

Table 2.2. Environmental Compliance and Package Information

Parameter	Value
Moisture sensitivity level (MSL)	3

Notes:

For additional product information not listed in the data sheet (e.g. RoHS Certifications, MSDS data, qualification data, REACH Declarations, ECCN codes, etc.), contact aeonsemi.com/contact_us

Table 2.3. Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Unit
Maximum operating temperature	T_{AMAX}	125	℃
Storage temperature	T_S	-55 - 125	℃
Supply voltage	V_{DD_MAX}	-0.5 - 3.8	V
Input voltage	V_{IN_MAX}	-0.5 - V_{DD}+0.3	V
ESD HBM (JESD22-A114)	HBM	4.0	kV
ESD CDM (JESD22-C101)	CDM	1.0	kV
Solder Temperature[2]	T_{PEAK}	260	℃
Solder time at T_{PEAK}[2]	T_P	20 - 40	sec

Notes:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. The device is compliant with JEDEC J-STD-020.

3. Package Outline Drawing

Figure 3.1. shows the package outline drawing for the AS5234 devices. Details of dimension for different size options are listed in Table 3.1.

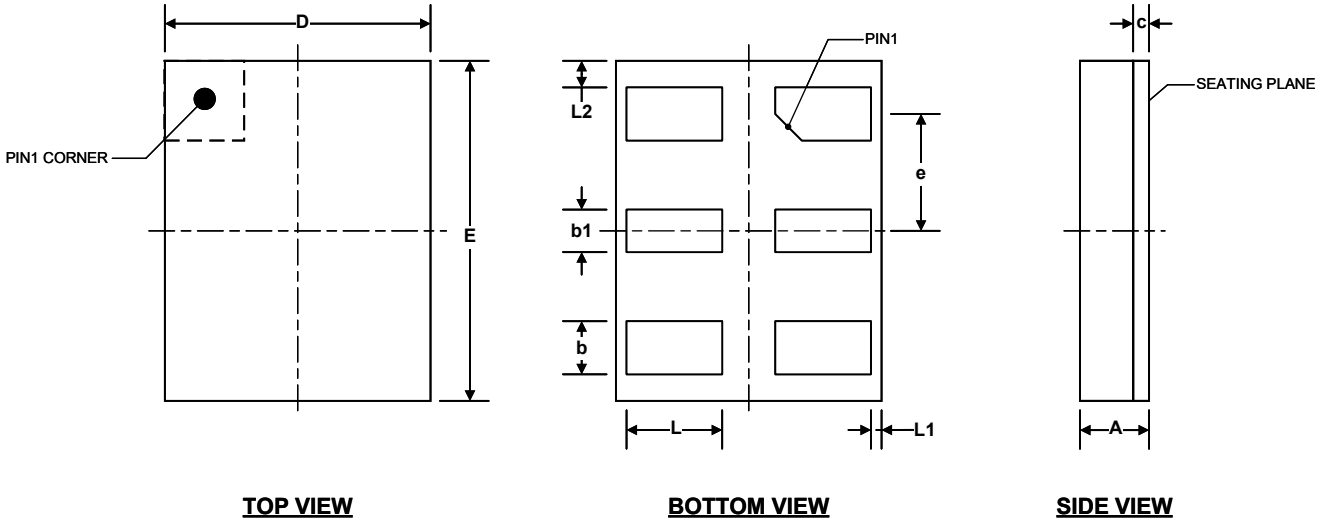


Figure 3.1. Package Outline Drawing

Table 3.1. Dimensions of Package Outline Drawing (mm)

Symbol	Min	Nom	Max
A	0.790	0.890	0.990
b	0.225	0.300	0.375
b1	0.225	0.300	0.375
D	1.550	1.600	1.650
e	–	0.750 BSC	–
E	1.950	2.000	2.050
L	0.375	0.450	0.525
L1	0.025	0.100	0.175

4. Recommended PCB Land Pattern

Figure 4.1. shows the drawing of recommended PCB land pattern for the AS5234 devices. Details of dimension for different size options are listed in Table 4.1.

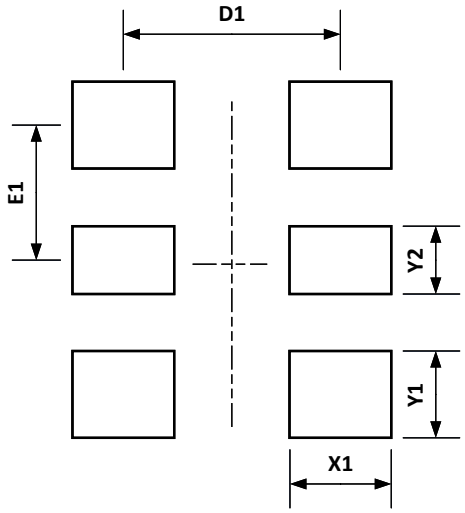


Figure 4.1. Recommended PCB Land Pattern

Table 4.1. Dimensions of Recommended PCB Land Pattern (mm)

Symbol	2016 Package
D1	1.05
E1	0.75
X1	0.75
Y1	0.50
Y2	0.50

Notes:

The following notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 0.8 1 for the pads.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

5. Top Mark

Figure 5.1. shows the top mark specifications for the AS5234 devices. Description of each line is listed in Table 5.1.

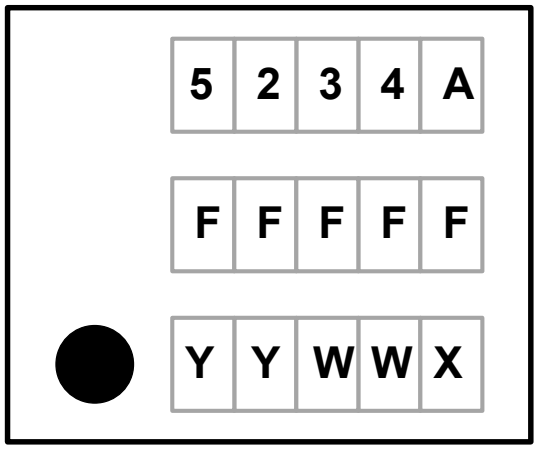


Figure 5.1. Top Mark

Table 5.1. Top Mark Description

Line	Position	Description
1	1-5	Device Name
2	1-5	Unique 5-digit Device Configuration Number
3	1	Pin 1 orientation mark (dot)
	2-3	Year (last two digits of the year), to be assigned by assembly site (ex: 2025 = 25)
	4-5	Calendar Work Week number (1-53), to be assigned by assembly site
	6	Manufacturer code

6. Packing Specification

Figure 6.1. shows the packing specifications for the AS5234 devices. Details of the tape specifications are listed in Table 6.1.
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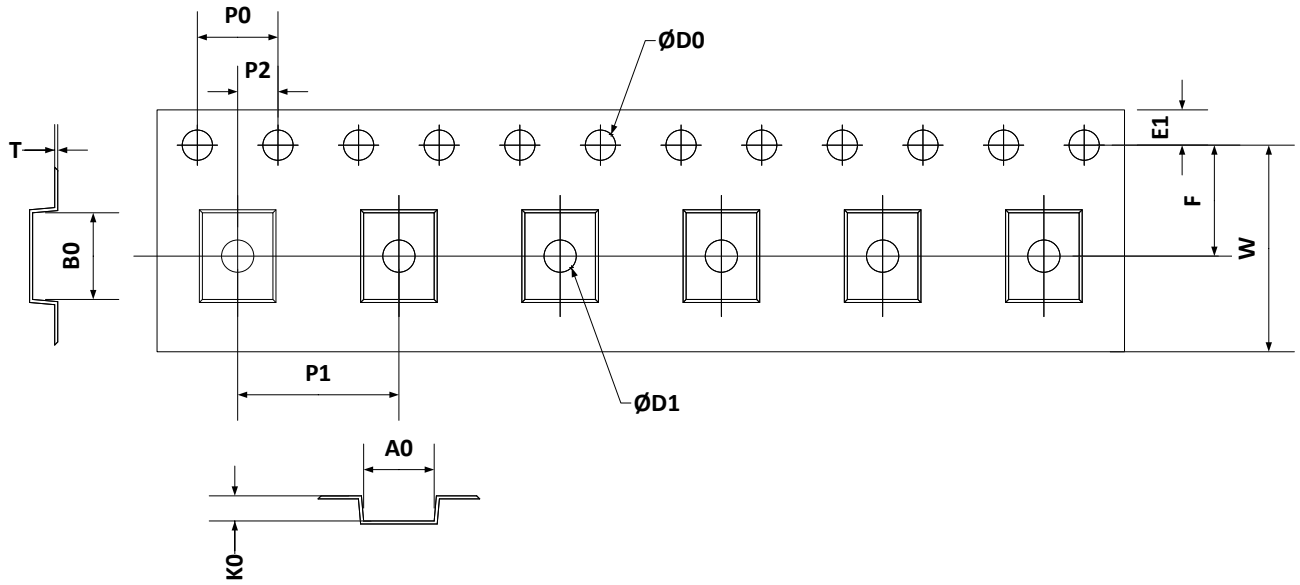

Figure 6.1. Tape Specification

Table 6.1. Dimensions of Tape (mm)

Symbol	2016 Package
A0	1.96 ± 0.05
B0	2.36 ± 0.05
K0	1.20 ± 0.05
E1	1.75 ± 0.10
F	3.50 ± 0.05
W	8.00 ± 0.10
T	0.25 ± 0.05
P0	4.00 ± 0.10
P1	4.00 ± 0.10
P2	2.00 ± 0.05
ϕD0	1.50 (+0.10/-0)
ϕD1	1.05 ± 0.10

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8. Revision History

Revision	Date	Description
1.06	Oct 2026	Updated ordering guide
1.05	Aug 2026	Removed paragraph first-line indentation Corrected top mark position table
1.03	Mar 2026	Updated the Top Mark Rule
1.02	Sep 2025	Corrected several description errors
1.01	Aug 2025	Officially release as mass production version
0.09	Feb 2025	Added 2016 package outline diagram
0.08	Aug 2024	Updated several items
0.07	Apr 2024	Remove the package outline drawings temporarily
0.06	Feb 2024	Updated the “Ordering Guide”
0.05	Aug 2023	Revised the stability for D-grade option
0.04	Jul 2023	Updated the package outline
0.03	Jun 2023	Updated the “Ordering Guide” and added phase noise jitter for clock >=100 MHz
0.02	Feb 2023	Updated the Temperature Stability Grade-D option
0.01	Nov 2021	Preliminary release