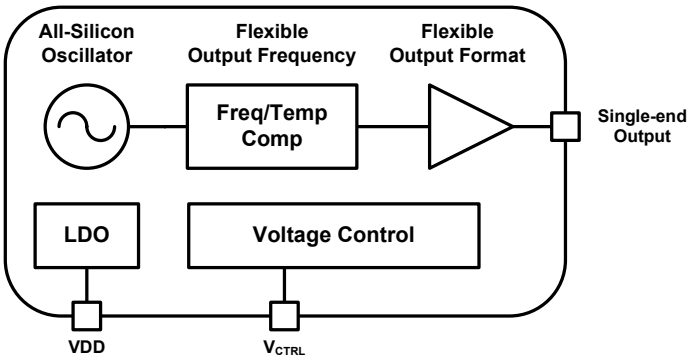
# AS5014 Automotive Grade LVCMOS Voltage Controlled Silicon Oscillator

## Description

The AS5014 all-silicon voltage-controlled oscillator utilizes digital frequency synthesis and sensing technologies to provide a quartz-free, MEMS-free, low-jitter voltage-controlled clock at any output frequency. With a factory-programmed center voltage and tuning slope, the AS5014 delivers an LVCMOS clock from 10 kHz to 125 MHz with 1 Hz resolution through Pin 1 (VC), the analog voltage-control input. It uses on-chip temperature and strain sensors, and an advanced LC tank architecture to achieve excellent reliability even in high-impact shock scenarios.

AS5014's on-chip power supply filtering provides ease of use in noisy systems with switched-mode power supplies. Offered in industry-standard 3225, 2520, and 2016 packages, the AS5014 has a dramatically simplified supply chain that enables Aeonsemi to ship samples shortly after receipt of order. Specific combinations of output frequency and voltage-control parameters are factory programmed at time of shipment, eliminating the long lead times associated with custom oscillators. This process also guarantees 100% electrical testing of every device before shipment.



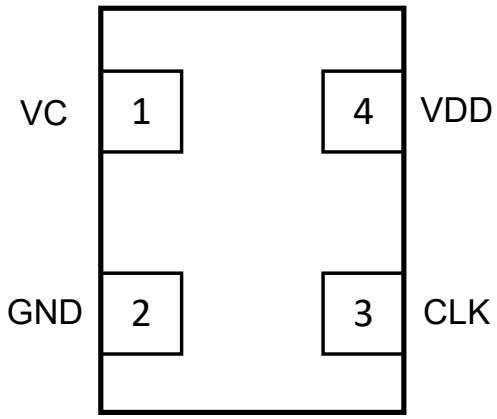

## Key Features

- Quartz-free and MEMS-free without mechanical moving parts
- LVCMOS output: 10 kHz to 125 MHz
- Low jitter: 1 ps Typ
  (12 kHz – 20 MHz, @125 MHz)
- Operating temperature range:
  - -40 to 85 ℃ (Industial grade)
  - -40 to 105 ℃ (Extended-Industial grade)
  - -40 to 125 ℃ (AEC-Q100 grade 1)
- Frequency tolerance: ±50 ppm (-40 to 125 ℃)
- Programmable tuning slope up to 250 ppm/V
- Immunity to shock and vibration
- Integrated LDO for on-chip power supply noise filtering
- Support 1.8V, 2.5V, 3.3V $V_{DD}$ supply operation
- Standard 3225, 2520 and 2016 packages

## Application

- IoT, Wearable device
- Medical, Industrial automation
- ADAS ECUs
- Automotive networking
- Lidar/Radar sensors
- Camera/Vision system

Pin definition




Top view

| Pin# | Description |
|---|---|
| 1 | VC = Voltage control input |
| 2 | GND = Ground |
| 3 | CLK = Clock output |
| 4 | VDD = Power supply |

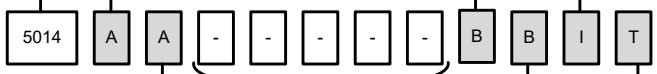
## 1. Ordering Guide

| XO Series | Description |
|---|---|
| 5014 | Voltage Control |

| | Device Type |
|---|---|
| A | General |
| B | Factory defined setting |

| | Package |
|---|---|
| B | 3225 |
| C | 2520 |
| D | 2016 |

| | Device Grade | Temperature Grade |
|---|---|---|
| I | Industrial grade | -40 to 85°C |
| E | Extended industrial grade | -40 to 105°C |
| A[2] | Automotive grade | -40 to 125°C |




| | Power Supply |
|---|---|
| A | 3.3 V |
| B | 2.5 V |
| C | 1.8 V |

| Configuration Code[1] | Description |
|---|---|
| xxxxx | Five digit numeric code |

The chip supports user-defined tuning slope and power supply voltage.
A unique five digit numeric code will be assigned for the specific combination of settings.

Device Revision

| Code | Packing type | Qty |
|---|---|---|
| T | 7-inch reel | 250 |
| R | 13-inch reel | 2500 |
| F | 13-inch reel | 5000 |
| <blank> | Bulk | Sample |

### Note:

1. The five-digit numeric code is an identification of the configurations. Check the datasheet appendix for the details.
2. Contact aeonsemi.com/contact_us for automotive grade option.

## 2. Electrical Specifications

**Table 2.1. Electrical Specifications**

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Operating Temperature Range | | | | | | |
| Temperature Range | $T_A$ | -40 | – | 85 | ℃ | Industrial grade |
| | | -40 | – | 105 | ℃ | Extended industrial grade |
| | | -40 | – | 125 | ℃ | Automotive AEC-Q100 Grade1 |
| Supply Voltage and Power Consumption | | | | | | |
| Supply Voltage | $V_{DD}$ | 1.62 | – | 3.63 | V | |
| Supply Current ($F_{CLK}$ = 25 MHz) | $I_{DD}$ | – | 10 | 11 | mA | Tristate Hi-Z (OE = 0) |
| | | – | 1 | 2 | mA | Ready State (ACT = 0) |
| | | – | 12 | 14 | mA | LVCMOS output ($C_L$=15pF) |
| Frequency Range | | | | | | |
| Frequency Range | $F_{CLK}$ | 0.01 | – | 125 | MHz | LVCMOS output |
| Frequency Tolerance | | | | | | |
| Total frequency tolerance | $F_{TOTAL}$ | -50 | – | 50 | ppm | -40 - 125℃ |
| **Notes:** Inclusive of initial frequency tolerance at 25℃, temperature stability over the corresponding operation temperature range, 10-year aging at 25℃ and variations over supply voltage, load and humidity after soldering-reflow shift settles. | | | | | | |
| VCXO Control Characteristics | | | | | | |
| Control voltage input | $V_C$ | 0 | – | $V_{DD}$ | V | Input reference voltage range |
| Center control voltage[1] | $V_{CEN}$ | – | $V_{DD}/2$ | – | V | Factory-programmable center voltage |
| Tuning slope[1] | $K_V$ | – | – | 250 | ppm/V | Factory-programmable tuning slope |
| Control voltage linearity | Lin | -3 | – | 3 | % | Linearity error |
| **Notes:** 1. The center control voltage and tuning slope are factory-programmable to meet application-specific requirements. Configurations can be customized at aeonsemi.com/AS5014/customize. | | | | | | |
| Output Characteristics | | | | | | |
| Powerup time | $T_{OSC}$ | – | – | 4 | ms | Time from power reaches 0.9 × $V_{DD}$ to output frequency ($F_{CLK}$) within spec |
| Duty cycle | DC | 45 | – | 55 | % | LVCMOS ($C_L$=15pF) |
| Rise/Fall time (20% to 80% VPP) | $T_{R/F}$ | – | 0.5 | 1.5 | ns | LVCMOS ($C_L$=15pF) |
| LVCMOS | $V_{OH}$ | 0.83×$V_{DD}$ | – | – | V | $C_L$=15pF |
| | $V_{OL}$ | – | – | 0.17×$V_{DD}$ | V | |
| Phase Noise and Jitter | | | | | | |
| RMS jitter BW: 12k - 20MHz | $R_J$ | – | 1 | 1.5 | ps | $F_{CLK}$ >= 100 MHz |
| | | – | 1.5 | 2 | ps | $F_{CLK}$ >= 25 MHz |
| Phase noise 125MHz LVCMOS output $V_{DD}$ = 1.8 - 3.3V | $PN_{1k}$ | – | -73 | – | dBc/Hz | Phase noise at 1kHz offset |
| | $PN_{10k}$ | – | -103 | – | dBc/Hz | Phase noise at 10kHz offset |
| | $PN_{100k}$ | – | -126 | – | dBc/Hz | Phase noise at 100kHz offset |
| | $PN_{1M}$ | – | -141 | – | dBc/Hz | Phase noise at 1MHz offset |
| | $PN_{10M}$ | – | -150 | – | dBc/Hz | Phase noise at 10MHz offset |

*Continued on next page*

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| PSNR | | | | | | |
| Spurs from power noise 50mV ripple $V_{DD}$ = 1.8V | PSNR | – | -76 | – | dBc | 100 kHz sine wave |
| | | – | -75 | – | dBc | 200 kHz sine wave |
| | | – | -75 | – | dBc | 500 kHz sine wave |
| | | – | -75 | – | dBc | 1 MHz sine wave |
| Spurs from power noise 50mV ripple $V_{DD}$ = 2.5 or 3.3V | PSNR | – | -83 | – | dBc | 100 kHz sine wave |
| | | – | -83 | – | dBc | 200 kHz sine wave |
| | | – | -83 | – | dBc | 500 kHz sine wave |
| | | – | -82 | – | dBc | 1 MHz sine wave |

**Table 2.2. Environmental Compliance and Package Information**

| Parameter | Value |
|---|---|
| Moisture sensitivity level (MSL) | 3 |

**Notes:**

For additional product information not listed in the data sheet (e.g. RoHS Certifications, MSDS data, qualification data, REACH Declarations, ECCN codes, etc.), contact aeonsemi.com/contact_us

**Table 2.3. Absolute Maximum Ratings[1]**

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Maximum operating temperature | $T_{AMAX}$ | 125 | ℃ |
| Storage temperature | $T_S$ | -55 - 125 | ℃ |
| Supply voltage | $V_{DD_MAX}$ | -0.5 - 3.8 | V |
| Input voltage | $V_{IN_MAX}$ | -0.5 - $V_{DD}$+0.3 | V |
| ESD HBM (JESD22-A114) | HBM | 4.0 | kV |
| ESD CDM (JESD22-C101) | CDM | 1.0 | kV |
| Solder Temperature[2] | $T_{PEAK}$ | 260 | ℃ |
| Solder time at $T_{PEAK}$[2] | $T_P$ | 20 - 40 | sec |

**Notes:**

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

## 3. Package Outline Drawing

Figure 3.1. shows the package outline drawing for the AS5014 devices. Details of dimension for different size options are listed in Table 3.1.

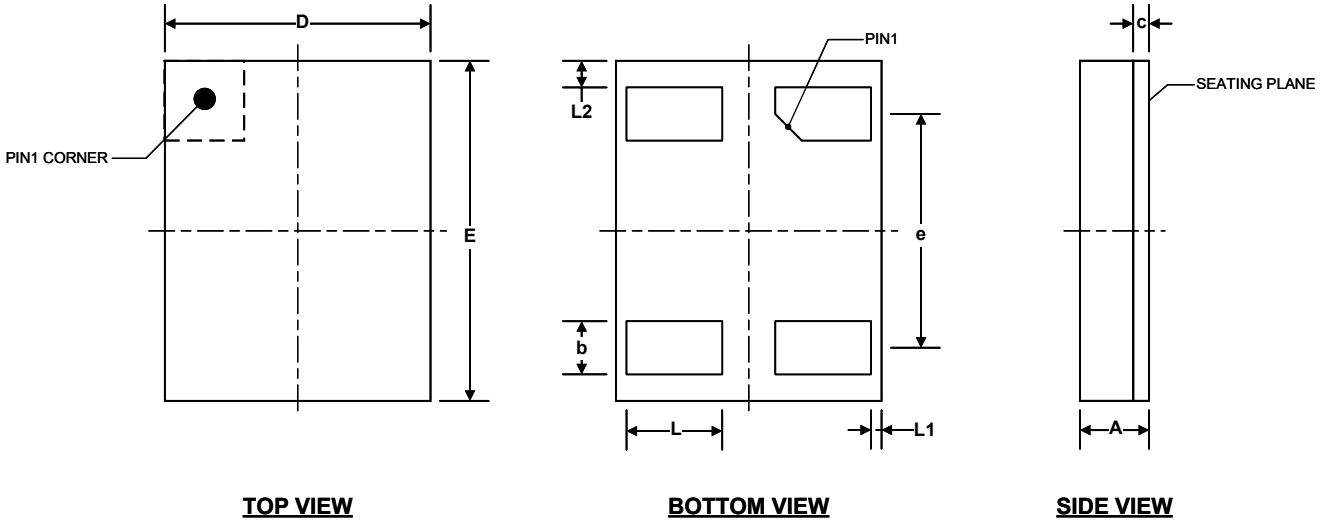



**Figure 3.1. Package Outline Drawing**

**Table 3.1. Dimensions of Package Outline Drawing (mm)**

| Symbol | 3225 Package | 2520 Package | 2016 Package |
|---|---|---|---|
| A | 0.85 ± 0.05 | 0.85 ± 0.05 | 0.75 ± 0.05 |
| b | 0.90 ± 0.05 | 0.55 ± 0.05 | 0.68 ± 0.10 |
| D | 2.50 ± 0.10 | 2.00 ± 0.10 | 1.60 ± 0.10 |
| e | 2.10 BSC | 1.75 BSC | 1.32 BSC |
| E | 3.20 ± 0.10 | 2.50 ± 0.10 | 2.00 ± 0.10 |
| L | 0.70 ± 0.05 | 0.45 ± 0.10 | 0.48 ± 0.05 |
| L1 | 0.10 ± 0.05 | 0.10 ± 0.05 | 0.10 ± 0.05 |

## 4. Recommended PCB Land Pattern

Figure 4.1. shows the drawing of recommended PCB land pattern for the AS5014 devices. Details of dimension for different size options are listed in Table 4.1.

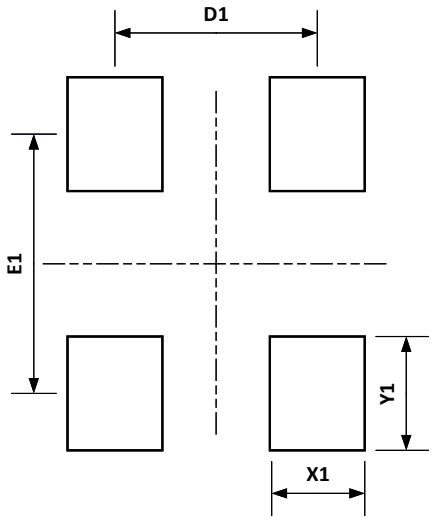



**Figure 4.1. Recommended PCB Land Pattern**

**Table 4.1. Dimensions of Recommended PCB Land Pattern (mm)**

| Symbol | 3225 Package | 2520 Package | 2016 Package |
|---|---|---|---|
| D1 | 1.70 | 1.45 | 1.02 |
| E1 | 2.10 | 1.75 | 1.32 |
| X1 | 1.00 | 0.75 | 0.78 |
| Y1 | 1.10 | 0.75 | 0.88 |

**Notes:**

The following notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 0.8 1 for the pads.

**Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 5. Top Mark

Figure 5.1. shows the top mark specifications for the AS5014 devices. Description of each line is listed in Table 5.1.

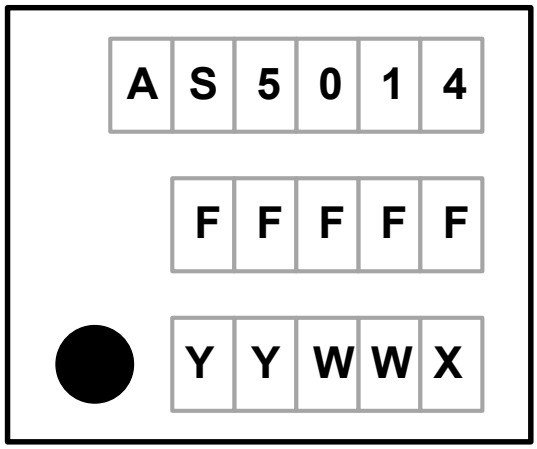



**Figure 5.1. Top Mark**

**Table 5.1. Top Mark Description**

| Line | Position | Description |
|---|---|---|
| 1 | 1-6 | Device Name |
| 2 | 1-5 | Unique 5-digit Device Configuration Number |
| 3 | 1 | Pin 1 orientation mark (dot) |
| | 2-3 | Year (last two digits of the year), to be assigned by assembly site (ex: 2025 = 25) |
| | 4-5 | Calendar Work Week number (1-53), to be assigned by assembly site |
| | 6 | Manufacturer code |

## 6. Packing Specification

Figure 6.1. shows the packing specifications for the AS5014 devices. Details of the tape specifications are listed in Table 6.1.
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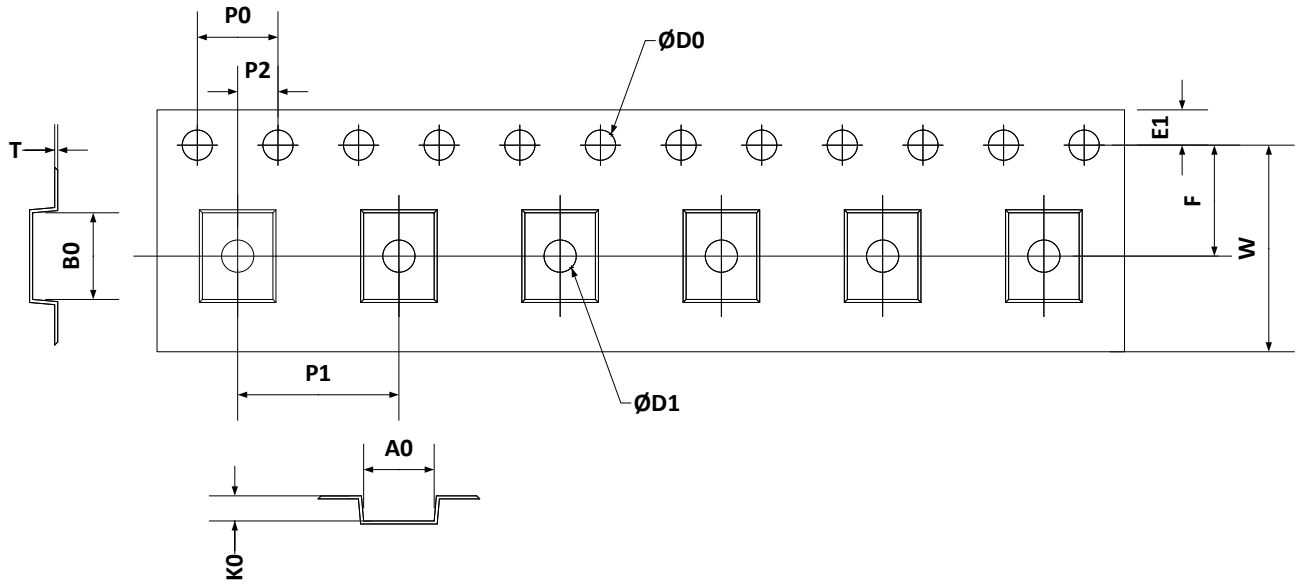


**Figure 6.1. Tape Specification**

**Table 6.1. Dimensions of Tape (mm)**

| Symbol | 3225 Package | 2520 Package | 2016 Package |
|---|---|---|---|
| A0 | 2.80 ± 0.10 | 2.30 ± 0.10 | 1.96 ± 0.05 |
| B0 | 3.50 ± 0.10 | 2.80 ± 0.10 | 2.36 ± 0.05 |
| K0 | 1.05 ± 0.10 | 1.30 ± 0.10 | 1.20 ± 0.05 |
| E1 | 1.75 ± 0.10 | 1.75 ± 0.10 | 1.75 ± 0.10 |
| F | 5.50 ± 0.05 | 5.50 ± 0.10 | 3.50 ± 0.05 |
| W | 12.00 ± 0.30 | 12.00 (+0.30/-0.10) | 8.00 ± 0.10 |
| T | 0.30 ± 0.05 | 0.30 ± 0.05 | 0.25 ± 0.05 |
| P0 | 4.00 ± 0.10 | 4.00 ± 0.10 | 4.00 ± 0.10 |
| P1 | 8.00 ± 0.10 | 8.00 ± 0.10 | 4.00 ± 0.10 |
| P2 | 2.00 ± 0.05 | 2.00 ± 0.10 | 2.00 ± 0.05 |
| $\phi$D0 | 1.50 ± 0.10 | 1.50 (+0.10/-0) | 1.50 (+0.10/-0) |
| $\phi$D1 | 1.60 ± 0.10 | 1.05 ± 0.10 | 1.05 ± 0.10 |

## 7. Important Notice and Disclaimer

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## 8. Revision History

| Revision | Date | Description |
|---|---|---|
| 1.02 | Oct 2026 | Updated ordering guide |
| 1.01 | Oct 2026 | Updated several items |
| 0.06 | Jan 2026 | Remove thermal stress section |
| 0.05 | Sep 2025 | Corrected several description errors |
| 0.04 | Jul 2025 | Updated the total stablity |
| 0.03 | Aug 2023 | Add package option 2016 |
| 0.02 | May 2023 | Updated the core power consumption |
| 0.01 | Nov 2022 | Initial release |