

AS512 Arcadium™ Pin Selectable Frequency CMOS Oscillator, 10 kHz to 212.5 MHz

The AS512 Arcadium™ all-silicon CMOS oscillator utilizes proprietary frequency synthesis and sensor technologies to provide a quartz-free, MEMS-free, low jitter clock at any output frequency. The device is factory-programmed to have 3 selectable frequencies ranging from 10 kHz to 212.5 MHz with < 0.026 ppb resolution and maintains low jitter across its operating range. It uses on-chip temperature and strain sensors, and an advanced LC tank architecture to achieve excellent reliabilities even in high impact shock scenarios.

AS512's on-chip power supply filtering provides industry-leading power supply noise rejection, simplifying the task of generating low jitter clocks in noisy systems that use switched-mode power supplies. Offered in an industry-standard 3225 and 5032 package, the AS512 has a dramatically simplified supply chain that enables Aeonsemi to ship samples shortly after receipt of order. Specific frequencies are factory programmed at time of shipment, eliminating the long lead times associated with custom frequencies. This process also guarantees 100% electrical testing of every device before shipment.

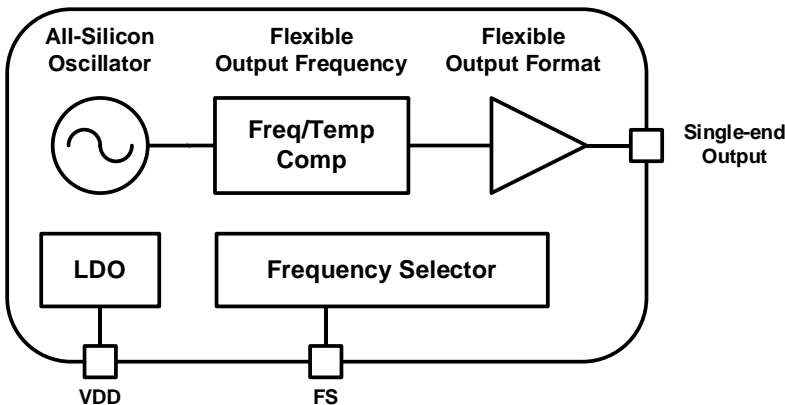


KEY FEATURES

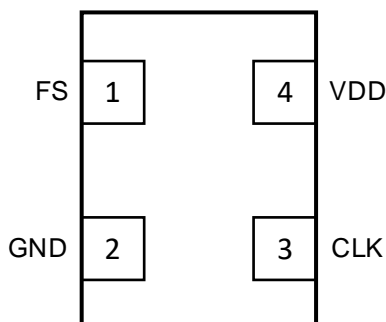
- Quartz-free and MEMS-free without mechanical moving parts
- CMOS compatible output
- Available with frequencies from 10 kHz to 212.5 MHz
- Low jitter: 350 fs Typ RMS (12 kHz – 20 MHz bandwidth)
- Temperature stability:
 - ± 20 ppm (-20 to 85 °C)
 - ± 35 ppm (-40 to 85 °C)
 - ± 35 ppm (-40 to 105 °C)
- Integrated LDO for on-chip power supply noise filtering
- Support 1.8V, 2.5V, 3.3V V_{DD} supply operation
- Industrial standard 3225 and 5032 package footprints

APPLICATIONS

- 1G/10G/40G/100G/200G Ethernet
- Servers, switches, storage, NICs, search acceleration
- Test and measurement
- Clock and data recovery
- FPGA/ASIC clocking



Pin Assignments

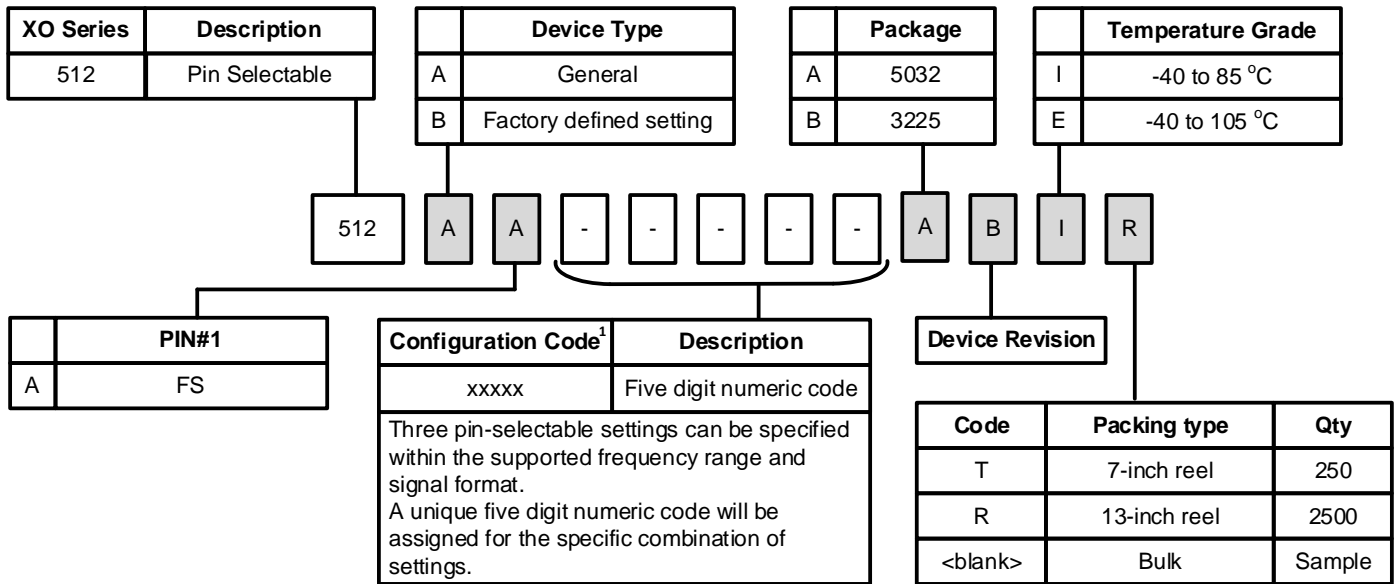


Top view
3225 package

Pin #	Descriptions
1	FS = Freq selector. Hi-z, High or Low
2	GND = Ground
3	CLK = Clock output
4	VDD = Power supply

1. Ordering Guide

The AS512 Oscillator supports up to 3 configurations selected by FS pin. Specific device configurations are programmed into the part at time of shipment, and samples are available in 2 weeks.



Notes:

1. The five-digit numeric code is an identification of the configurations. Check the datasheet appendix for the details

2. Control Pins

2.1. Overview

The AS512 is a pin selectable oscillator that generates reference clocks with any output frequencies (10 kHz – 212.5 MHz) CMOS clock, Pin#1 of AS512 is designed as frequency select (FS).

2.2. Configuration Selection

The on chip Non-Volatile Memory (NVM) stores three pre-programmed output frequencies. It selects an output frequency using the frequency select pin (FS). Configurations can be preset at aeonsemi.com/as512/customize.

Table 2.1. shows an example of a configuration.

Table 2.1. A Configuration Example with 3 Pre-Programmed Presets

Preset	FS (Pin 1)	Output Frequency
1	Low	27 MHz
2	Hi-Z	100 MHz
3	High	50 MHz

Notes:

AS512 supports options of VCXO and SSC (Spread Spectrum Clock) feature on the control pin.

Contact aeonsemi.com/contact-us/ for the advanced configurations.

3. Electrical Specifications

Table 3.1. Electrical Specifications

$V_{DD} = 1.8\text{ V}, 2.5\text{ or }3.3\text{ V} \pm 5\%$, $T_A = -40\text{ to }105\text{ }^\circ\text{C}$

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Temperature Range	T_A		-40	—	105	$^\circ\text{C}$
Frequency Range		CMOS	0.01	—	212.5	MHz
Supply Voltage	V_{DD}		1.71		3.47	V
Supply Current ($F_{CLK} = 50\text{ MHz}$)	I_{DD}	Tristate Hi-Z ($OE = 0$)	—	40	50	mA
		Ready State ($ACT = 0$)	—	1	2	mA
		CMOS ($C_L = 15\text{ pF}$)	—	40	55	mA
Temperature Stability ¹	F_{STAB}	-20 to +85 $^\circ\text{C}$	-20	—	+20	ppm
		-40 to +85 $^\circ\text{C}$	-35	—	+35	ppm
		-40 to +105 $^\circ\text{C}$	-35	—	+35	ppm
Frequency offset ²	F_{OFFSET}	At 25 $^\circ\text{C}$	-15	—	+15	ppm
Rise/Fall Time (20% to 80% V_{PP})		CMOS ($C_L = 15\text{ pF}$)	—	0.5	1.5	ns
Duty Cycle	DC	CMOS ($C_L = 15\text{ pF}$)	45	—	55	%
Frequency select (FS) ³	V_{IH}		$0.7 \times V_{DD}$	—	—	V
	V_{IL}		—	—	$0.3 \times V_{DD}$	V
Powerup Time	T_{OSC}	Time from $0.9 \times V_{DD}$ until output frequency (F_{CLK}) within spec	—	—	4	ms
CMOS Output	V_{OH}	$I_{OH} = 8/6/4\text{ mA}$ for 3.3/2.5/1.8V V_{DD}	$0.83 \times V_{DD}$	—	—	V
	V_{OL}	$I_{OL} = 8/6/4\text{ mA}$ for 3.3/2.5/1.8V V_{DD}	—	—	$0.17 \times V_{DD}$	V

Notes:

1. Frequency / temperature characteristics with offset removed.
2. Inclusive of initial frequency tolerance at 25 $^\circ\text{C}$, 10-year aging at 25 $^\circ\text{C}$, and variations over supply voltage, load and humidity after soldering-reflow shift settles.
3. FS includes a 50 k Ω pull-up to V_{DD} and a 50 k Ω pull-down to GND.

Table 3.2. Clock Output Phase Jitter and PSRR

V_{DD} = 1.8 V, 2.5 or 3.3 V ± 5%, T_A = -40 to 105 °C

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Phase Jitter (RMS, 12 kHz - 20 MHz) ^{1,2} F _{CLK} ≥ 10 MHz	φ _J	CMOS	—	350	—	fs
Spurs Induced by External Power Supply Noise, 50 mV _{pp} Ripple. CMOS 125 MHz Output V _{DD} = 1.8 V	PSRR	100 kHz sine wave	—	-76	—	dBc
		200 kHz sine wave	—	-75	—	
		500 kHz sine wave	—	-75	—	
		1 MHz sine wave	—	-75	—	
Spurs Induced by External Power Supply Noise, 50 mV _{pp} Ripple. CMOS 125 MHz Output V _{DD} = 2.5 or 3.3 V	PSRR	100 kHz sine wave	—	-83	—	dBc
		200 kHz sine wave	—	-83	—	
		500 kHz sine wave	—	-83	—	
		1 MHz sine wave	—	-82	—	

Notes:

1. Applies to output frequency: 50, 100, 125 MHz.
2. Guaranteed by characterization. Jitter inclusive of any spurs.

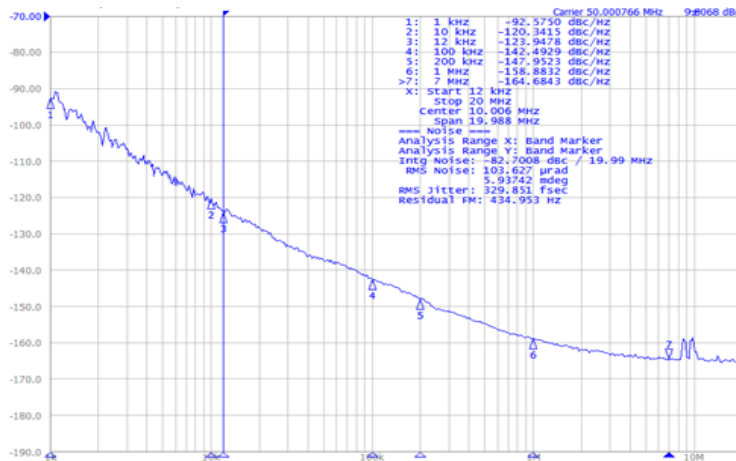


Figure 3.1. Phase Noise at 50 MHz

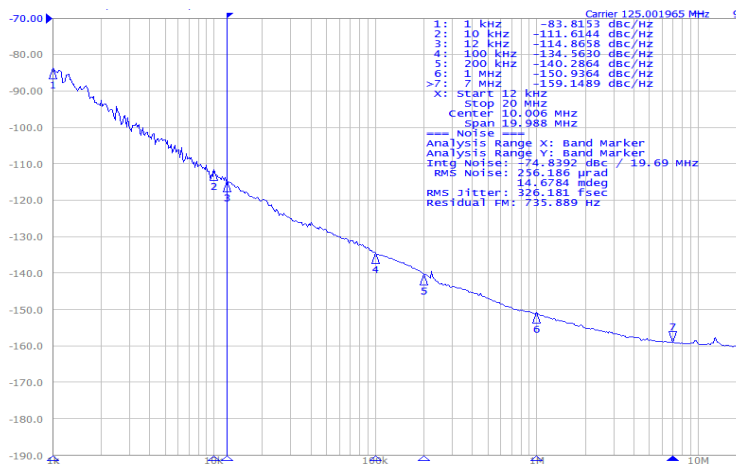


Figure 3.2. Phase Noise at 125 MHz

Table 3.3. Environmental Compliance and Package Information

Parameter	Test Condition
Moisture Sensitivity Level	2

Notes:

For additional product information not listed in the data sheet (e.g. RoHS Certifications, MSDS data, qualification data, REACH Declarations, ECCN codes, etc.), contact aeonsemi.com/contact_us

Table 3.4. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air	108	°C/W
Thermal Resistance Junction to Board	Θ_{JB}	Still Air	84	°C/W
Max Junction Temperature	T_J	Still Air	125	°C

Table 3.5. Absolute Maximum Ratings¹

Parameter	Symbol	Rating	Unit
Maximum Operating Temp	T_{AMAX}	105	°C
Storage Temperature	T_S	-55 to 105	°C
Supply Voltage	V_{DD}	-0.5 to 3.8	V
Input Voltage	V_{IN}	-0.5 to $V_{DD} + 0.3$	V
ESD HBM (JESD22-A114)	HBM	4.0	kV
ESD CDM (JESD22-C101)	CDM	1.0	kV
Solder Temperature ²	T_{PEAK}	260	°C
Solder Time at T_{PEAK} ²	T_P	20 - 40	sec

Notes:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. The device is compliant with JEDEC J-STD-020.

4. Package Outline

4.1. Package Outline (5032)

The figure below illustrates the package details for the AS512. The table below lists the values for the dimensions shown in the illustration.

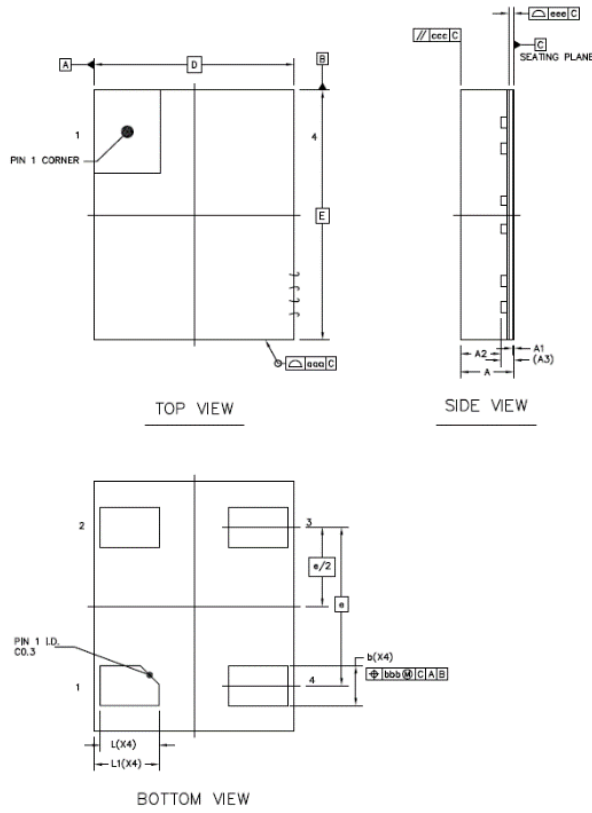


Figure 4.1. AS512 5032 Package Outline Diagram

Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	0.8	0.85	0.9
A1	0	0.02	0.05
A2	—	0.65	—
A3	0.203 REF		
b	0.59	0.64	0.69
D	3.2 BSC		
E	4 BSC		
e	2.54 BSC		
L	0.89	0.94	0.99
L1	1.04 REF		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

4.2. Package Outline (3225)

The figure below illustrates the package details for the AS512. The table below lists the values for the dimensions shown in the illustration.

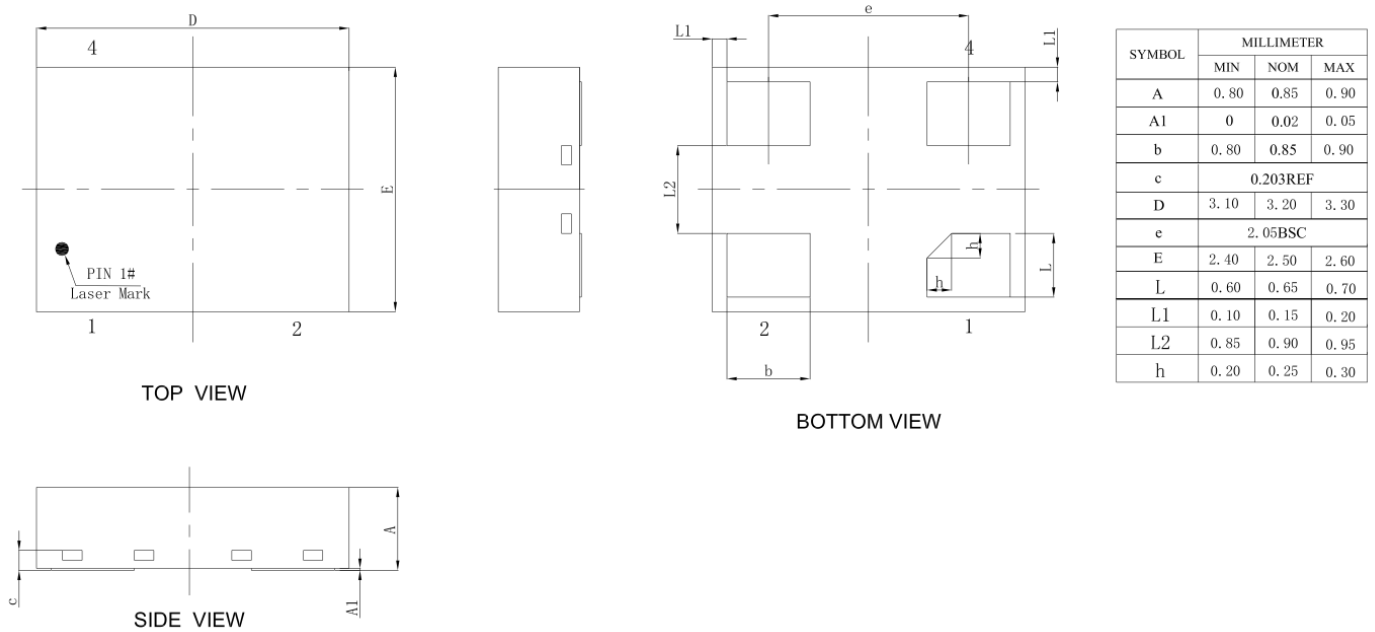


Figure 4.2. AS512 3225 Package Outline Diagram

Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	0.8	0.85	0.9
A1	0	0.02	0.05
b	0.80	0.85	0.90
c	0.203 REF		
D	3.10	3.20	3.30
e	2.05 BSC		
E	2.40	2.50	2.60
L	0.60	0.65	0.70
L1	0.10	0.15	0.20
L2	0.85	0.90	0.95
h	0.20	0.25	0.30

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

5. PCB Land Pattern

The figure below illustrates the PCB land pattern for the AS512. The table below lists the values for the dimensions shown in the illustration.

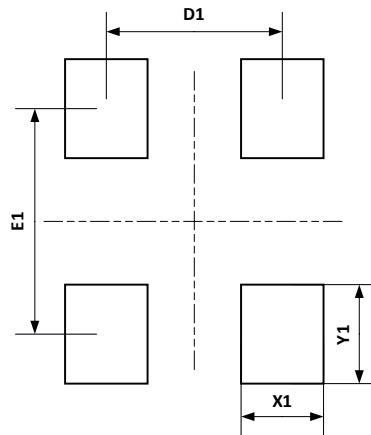


Figure 5.1. AS512 PCB Land Pattern

PCB Land Pattern Dimensions (mm)

Dimension	Description	5032 Package Value (mm)	3225 Package Value (mm)
X1	Width - leads on long sides	1.00	0.70
Y1	Height - leads on long sides	0.70	0.90
D1	Pitch in X directions of XLY1 leads	2.06	1.60
E1	Lead pitch XLY1 leads	2.54	2.05

Notes:

The following notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 0.8:1 for the pads.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6. Top Marking

The figure below illustrates the mark specification for the AS512. The table below lists the line information.

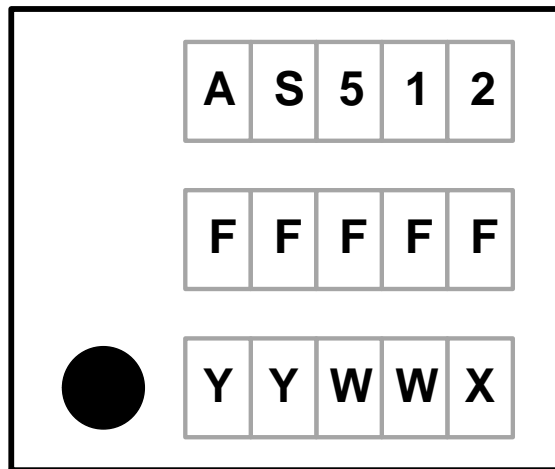


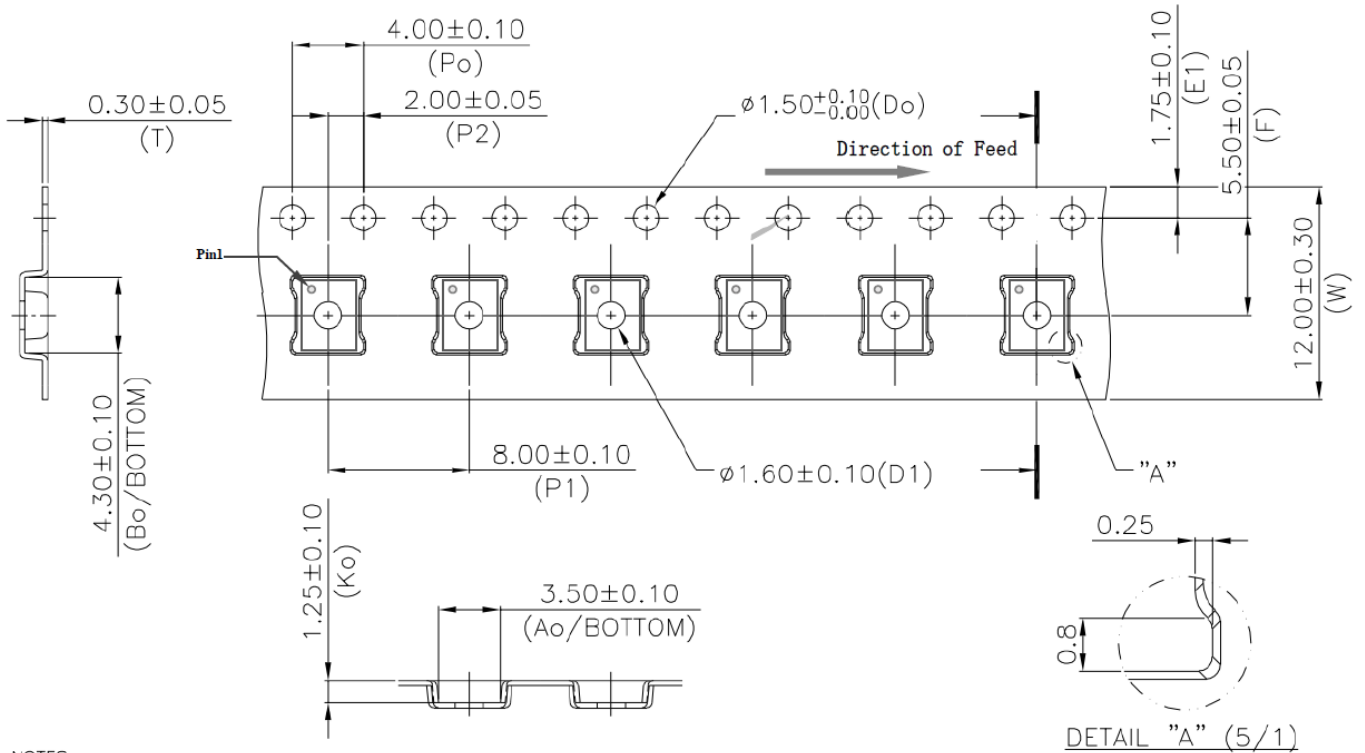
Figure 6.1. AS512 Top Mark

Table 6.1. AS512 Top Mark Description

Line	Position	Description
1	1-5	Device Name
2	1-5	Unique 5-digit Device Configuration Number
3	Position 1	Pin 1 orientation mark (dot)
	Position 2-3	Year (last two digits of the year), to be assigned by assembly site (ex: 2017 = 17)
	Position 4-5	Calendar Work Week number (1-53), to be assigned by assembly site
	Position 6	Assembly site code

7. Packing specification

7.1. Tape & Reel (5032)

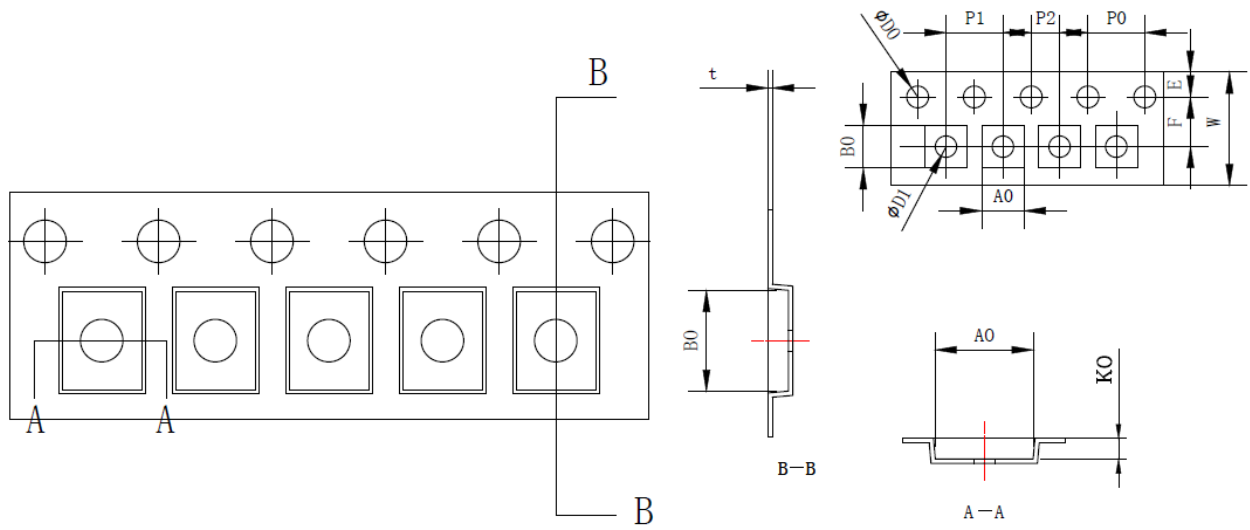


NOTES:

1. DIM IN mm.
2. 10 SPROCKET HOLE PITCHES CUMULATIVE TOLERANCE ± 0.20 mm.
3. CAMBER NOT TO EXCEED 1 mm IN 250 mm.
4. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
5. (S.R. ohms/sq.) MEANS SURFACE RESISTIVITY OF THE CARRIER TAPE. (EIA-541 STANDARD)
6. DIMENSIONS IN ACCORDANCE WITH EIA-481 SPECIFICATIONS.

Figure 7.1. AS512 5032 Package Packing Specification

7.2. Tape & Reel (3225)



W	E	F	D0	D1	P0	P2	10P0	P1	A0	A1	B0	B1	K0	K1	t
8.00	1.75	3.50	1.50	1.00	4.00	2.00	40.00	4.00	2.80	/	3.60	/	1.10	/	0.30
±0.30	±0.10	±0.05	+0.10	+0.10	±0.10	±0.10	±0.20	±0.10	±0.10	/	±0.10	/	±0.10	/	±0.05

Figure 7.2. AS512 3225 Package Packing Specification

8. IMPORTANT NOTICE AND DISCLAIMER

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9. Revision History

Rev	Date	Description
1.12	Aug 2024	Add packing specification
1.11	Mar 2024	Updated the frequency offset
1.10	Jul 2022	Updated the top mark specification
1.01	Dec 2021	Adjusted the PCB land pattern dimensions
1.00	Sep 2021	With certain specification update
0.95	Jun 2021	Corrected the Ordering Guide Insert -40~105oC temperature range option Insert section "IMPORTANT NOTICE AND DISCLAIMER"
0.2	Mar 2021	Changed the frequency range and ordering guide
0.1	Feb 2021	Initial release