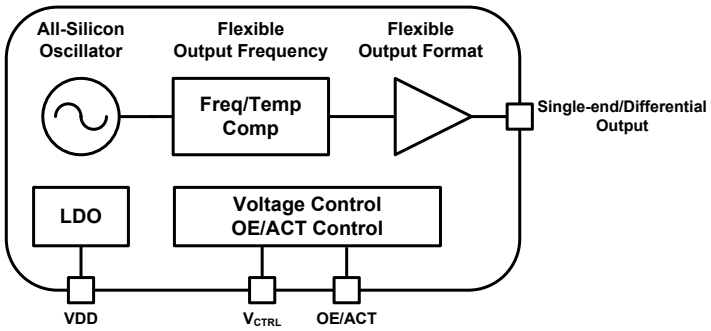
AS5004 Low Jitter Differential Voltage Controlled Silicon Oscillator

Description

The AS5004 Arcadium™ all-silicon differential oscillator utilizes proprietary frequency synthesis and sensor technologies to provide a quartz-free, MEMS-free, low-jitter voltage-controlled clock at any output frequency. The device is factory-programmed to output differential frequencies ranging from 10 kHz to 350 MHz with 1 Hz resolution, and the center control voltage and tuning slope are factory-programmed according to the ordering configuration. The AS5004 uses on-chip temperature and strain sensors, and an advanced LC tank architecture to achieve excellent reliability even in high-impact shock scenarios.

AS5004's on-chip power supply filtering provides industry-leading power supply noise rejection, simplifying the task of generating low-jitter clocks in noisy systems that use switched-mode power supplies. Offered in a variety of industry-standard packages, the AS5004 has a dramatically simplified supply chain that enables Aeonsemi to ship samples shortly after receipt of order. Specific combinations of output frequency and voltage-control parameters are factory-programmed at time of shipment, eliminating the long lead times associated with custom oscillators. This process also guarantees 100% electrical testing of every device before shipment.



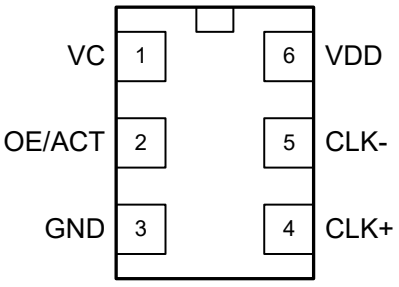
Key Features

- Quartz-free and MEMS-free without mechanical moving parts
- LVCMOS output: 10 kHz to 212.5 MHz
- Differential output: 10 kHz to 350 MHz
- Low jitter: 350 fs Typ
  (12 kHz –20 MHz, @156.25 MHz)
- Compliant to PCIe Gen 1/2/3/4/5/6 jitter spec
- Temperature stability:
  - ±20 ppm (-20 to 85 ℃)
  - ±35 ppm (-40 to 85 ℃)
  - ±35 ppm (-40 to 105 ℃)
- Programmable tuning slope up to 250 ppm/V
- Integrated LDO for on-chip power supply noise filtering
- Support 1.8V, 2.5V, 3.3V V_{DD} supply operation
- Industrial standard 3225 and 5032 package footprints

Application

- 1G/10G/40G/100G/200G Ethernet
- Servers, switches, storage, NICs
- Test and measurement
- Clock and data recovery
- FPGA/ASIC clocking

Pin definition



Top view

Pin#	Description
1	VC = Voltage control input
2	OE = Output enable. Active high ACT = Device active. Active high
3	GND = Ground
4	CLK+ = Clock output
5	CLK- = Complementary clock output
6	VDD = Power supply

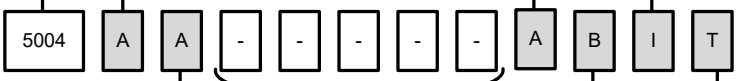
1. Ordering Guide

XO Series	Description
5004	Voltage Control

	Device Type
A	General
B	Factory defined setting

	Package
A	5032
B	3225
C	2520

	Temperature Grade
I	-40 to 85 °C
E	-40 to 105 °C



	Power supply
A	3.3 V
B	2.5 V
C	1.8 V

Configuration Code[1]	Description
xxxxx	Five digit numeric code

The chip supports user-defined tuning slope and power supply voltage.

A unique five digit numeric code will be assigned for the specific combination of settings.

Device Revision

Code	Packing type	Qty
T	7-inch reel	250
R	13-inch reel	2500
F	13-inch reel	5000
<blank>	Bulk	Sample

Note:

1. The five-digit numeric code is an identification of the configurations. Check the datasheet appendix for the details.

2. Electrical Specifications

Table 2.1. Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
Operating Temperature Range						
Temperature Range	T_A	-40	–	85	℃	Industrial grade
		-40	–	105	℃	Extended industrial grade
Supply Voltage and Power Consumption						
Supply Voltage	V_{DD}	1.62	–	3.63	V	
Supply Current (F_{CLK} = 156.25 MHz)	I_{DD}	–	40	50	mA	Tristate Hi-Z (OE = 0)
		–	1	2	mA	Ready State (ACT = 0)
		–	70	80	mA	LVPECL (Standard)
		–	60	70	mA	LVPECL (Self-Biased)
		–	45	55	mA	LVDS
		–	60	70	mA	HCSL
		–	60	70	mA	CML
		–	40	55	mA	Single LVCMOS (C_L=15pF)
		–	60	70	mA	Dual LVCMOS (C_L=15pF)
Frequency Range						
Frequency Range	F_{CLK}	0.01	–	212.5	MHz	LVCMOS output
		0.01	–	350	MHz	Differential output
Frequency Tolerance						
Initial frequency accuracy	F_{INIT}	-10	–	10	ppm	Inclusive of initial frequency tolerance at 25℃ and variations over supply voltage, load and humidity after soldering-reflow shift settles.
Temperature stability	F_{STAB}	-20	–	20	ppm	-20 - 85℃
		-35	–	35	ppm	-40 - 85℃
		-35	–	35	ppm	-40 - 105℃
Aging	F_{AGING}	-5	–	5	ppm	10 Year at 25 ℃
VCXO Control Characteristics						
Control voltage input	V_C	0	–	V_{DD}	V	Input reference voltage range
Center control voltage[3]	V_{CEN}	–	$V_{DD}/2$	–	V	Factory-programmable center voltage
Tuning slope[3]	K_V	–	–	250	ppm/V	Factory-programmable tuning slope
Control voltage linearity	Lin	-3	–	3	%	Linearity error

Notes:

3. The center control voltage and tuning slope are factory-programmable to meet application-specific requirements. Configurations can be customized at aeonsemi.com/AS5004/customize.

Continued on next page

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output Characteristics						
Powerup time	T_{OSC}	–	–	4	ms	Time from power reaches 0.9 × V_{DD} to output frequency (F_{CLK}) within spec
Duty cycle	DC	45	–	55	%	All formats
Rise/Fall time (20% to 80% VPP)	$T_{R/F}$	–	0.5	1.5	ns	LVCMOS (C_L=15pF)
		–	–	350	ps	LVPECL / LVDS / CML
		–	–	550	ps	HCSL
LVPECL (Standard)	V_{OC}	V_{DD}-1.55	V_{DD}-1.4	V_{DD}-1.25	V	Mid-level
	V_O	1.35	1.6	1.85	V_{PP}	Swing (Diff)
LVPECL (Self-Biased)	V_O	1.35	1.6	1.85	V_{PP}	Swing (Diff)
LVDS	V_{OC}	1.125	1.20	1.275	V	Mid-level (2.5V, 3.3V V_{DD})
		0.78	0.85	0.92	V	Mid-level (1.8V V_{DD})
	V_O	0.64	0.8	0.96	V_{PP}	Swing (Diff)
HCSL (R_{TERM} = 50 Ω)	V_{OC}	0.35	0.4	0.45	V	Mid-level
	V_O	1.28	1.6	1.92	V_{PP}	Swing (Diff)
HCSL (R_{TERM} = 42.5 Ω)	V_{OC}	0.35	0.4	0.45	V	Mid-level
	V_O	1.29	1.62	1.94	V_{PP}	Swing (Diff)
CML	V_{OC}	V_{DD}-0.35	V_{DD}-0.4	V_{DD}-0.45	V	Mid-level
	V_O	1.28	1.6	1.92	V_{PP}	Swing (Diff)
LVCMOS	V_{OH}	0.83×V_{DD}	–	–	V	C_L=15pF
	V_{OL}	–	–	0.17×V_{DD}	V	
Phase Noise and Jitter						
RMS jitter BW 12kHz to 20MHz	R_J	–	350	750	fs	F_{CLK} >= 100 MHz
		–	450	750	fs	F_{CLK} >= 25 MHz
RMS jitter 156.25 MHz LVDS output	R_{J_156M25}	–	322	400	fs	BW 12kHz to 20MHz
		–	48	60	fs	BW 4MHz to 16MHz
		–	53	60	fs	BW 4MHz to 20MHz
RMS jitter 312.5 MHz LVDS output	R_{J_312M5}	–	357	400	fs	BW 12kHz to 20MHz
		–	36	50	fs	BW 4MHz to 16MHz
		–	40	50	fs	BW 4MHz to 20MHz
Phase noise 156.25 MHz LVDS output V_{DD} = 1.8 - 3.3 V	PN_{1k}	–	-80	–	dBc/Hz	Phase noise at 1 kHz offset
	PN_{10k}	–	-110	–	dBc/Hz	Phase noise at 10 kHz offset
	PN_{100k}	–	-133	–	dBc/Hz	Phase noise at 100 kHz offset
	PN_{1M}	–	-152	–	dBc/Hz	Phase noise at 1 MHz offset
	PN_{10M}	–	-161	–	dBc/Hz	Phase noise at 10 MHz offset
PSRR						
Spurs from power noise 50mV ripple V_{DD} = 1.8V	PSRR	–	-76	–	dBc	100 kHz sine wave
		–	-75	–	dBc	200 kHz sine wave
		–	-75	–	dBc	500 kHz sine wave
		–	-75	–	dBc	1 MHz sine wave
Spurs from power noise 50mV ripple V_{DD} = 2.5 or 3.3V	PSRR	–	-83	–	dBc	100 kHz sine wave
		–	-83	–	dBc	200 kHz sine wave
		–	-83	–	dBc	500 kHz sine wave
		–	-82	–	dBc	1 MHz sine wave

Table 2.2. PCIe Clock Output Performance (100MHz HCSL)

Parameter	Specification	Max	Unit	Test Condition
PCIe Gen 1.1	N/A	0.311	ps	Includes PLL BW 1.5 - 22 MHz Peaking = 3dB, T_D=10 ns
PCIe Gen 2.1	3.1	0.022	ps	Includes PLL BW 5MHz & 8 - 16 MHz Peaking = 0.01 - 1 dB & 3 dB, T_D=12ns Low Band, F $<$ 1.5 MHz
	3.0	0.259	ps	Includes PLL BW 5MHz & 8 - 16 MHz Peaking = 0.01 - 1 dB & 3 dB, T_D=12ns High Band, 1.5 MHz $<$ F $<$ Nyquist
PCIe Gen 3.0 common clock	1	0.085	ps	Includes PLL BW 2 - 4 MHz & 5 MHz Peaking = 0.01 - 2dB & 1dB, T_D=12 ns CDR = 10 MHz
PCIe Gen 4.0 common clock	0.5	0.085	ps	Includes PLL BW 2 - 4 MHz & 5 MHz Peaking = 0.01 - 2dB & 1dB, T_D=12 ns CDR = 10 MHz
PCIe Gen 5.0 common clock	0.15	0.033	ps	Includes PLL BW 500 kHz - 1.8 MHz Peaking = 0.01 – 2dB, T_D=12 ns CDR = 20 MHz
PCIe Gen 6.0 common clock	0.1	0.021	ps	Includes PLL BW 500 kHz – 1 MHz Peaking = 0.01 – 2dB, T_D=12 ns CDR = 10 MHz

Class	Data Rate	Architecture	Specs	Max HF RMS	Max LF RMS	Max Pk-Pk	Compliance Summary
GEN1	2.5 Gb/s	Common Clock	1.1 2.1 3.1	310.77 fs	41.59 fs	N/A	N/A
GEN2	5 Gb/s	Common Clock	1.1 2.1 3.1	259.42 fs	21.89 fs	N/A	All PASS
GEN3	8 Gb/s	Common Clock	3.1 4.0	84.54 fs	4.68 fs	N/A	All PASS
GEN4	16 Gb/s	Common Clock	4.0	84.54 fs	4.68 fs	N/A	All PASS
GEN5	32 Gb/s	Common Clock	5.0	32.92 fs	2.09 fs	N/A	All PASS
GEN6	64 Gb/s	Common Clock	6.0	21.00 fs	0.88 fs	N/A	All PASS

Figure 2.1. PCI-Express clock Compliance Summary

Table 2.3. Environmental Compliance and Package Information

Parameter	Value
Moisture sensitivity level (MSL)	1

Notes:

For additional product information not listed in the data sheet (e.g. RoHS Certifications, MSDS data, qualification data, REACH Declarations, ECCN codes, etc.), contact aeonsemi.com/contact_us

Table 2.4. Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Unit
Maximum operating temperature	T_{AMAX}	125	℃
Storage temperature	T_S	-55 - 125	℃
Supply voltage	V_{DD_MAX}	-0.5 - 3.8	V
Input voltage	V_{IN_MAX}	-0.5 - V_{DD}+0.3	V
ESD HBM (JESD22-A114)	HBM	4.0	kV
ESD CDM (JESD22-C101)	CDM	1.0	kV
Solder Temperature[2]	T_{PEAK}	260	℃
Solder time at T_{PEAK}[2]	T_P	20 - 40	sec

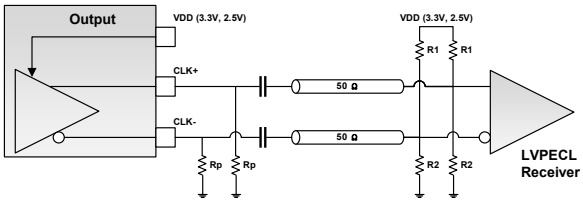
Notes:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

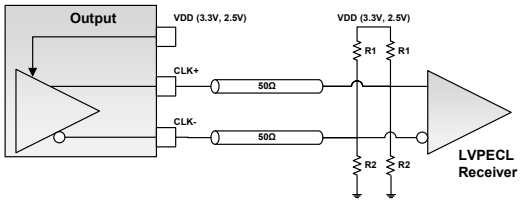
3. Recommended Output Terminations

3.1. Differential Output

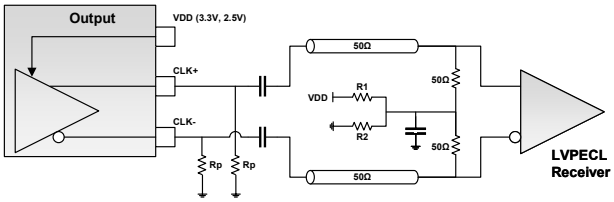
The output drivers support AC-coupled or DC-coupled terminations as shown in figures below.



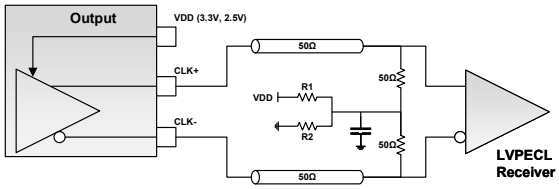
AC-Coupled LVPECL - Thevenin Termination



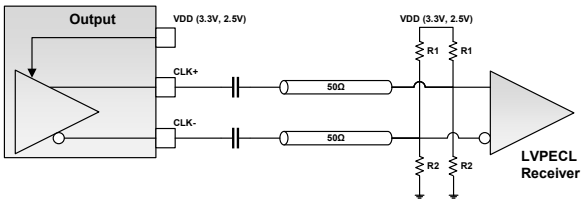
DC-Coupled LVPECL - Thevenin Termination



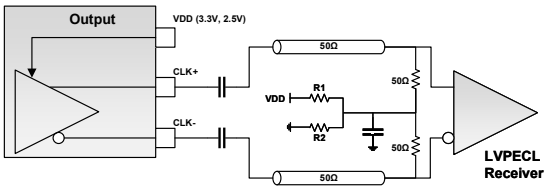
AC-Coupled LVPECL - 50 Ω with VTT Bias



DC-Coupled LVPECL - 50 Ω with VTT Bias



AC-Coupled Self-Biased LVEPCL - Thevenin Termination



AC-Coupled Self-Biased LVEPCL - 50 Ω with VTT Bias

Figure 3.1. LVPECL Output Terminations

Table 3.1. LVPECL Termination Resistor Values

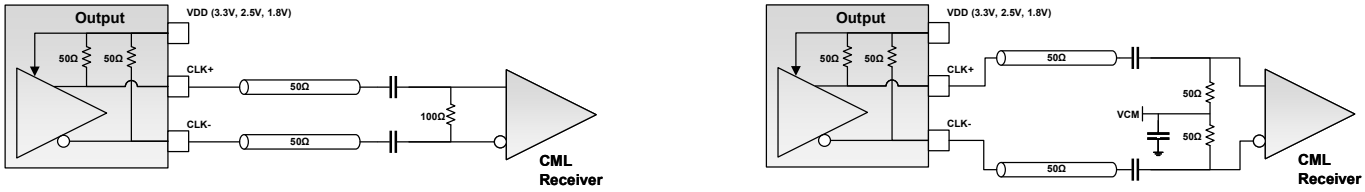
AC Coupled LVPECL Termination Resistor Values			
V_{DD}(V)	R_P	R_1	R_2
3.3 V	158 Ω	127 Ω	82.5 Ω
2.5 V	92 Ω	250 Ω	62.5 Ω

DC Coupled LVPECL Termination Resistor Values		
V_{DD}(V)	R_1	R_2
3.3 V	127 Ω	82.5 Ω
2.5 V	250 Ω	62.5 Ω

AC-Coupled LVDS

DC-Coupled LVDS

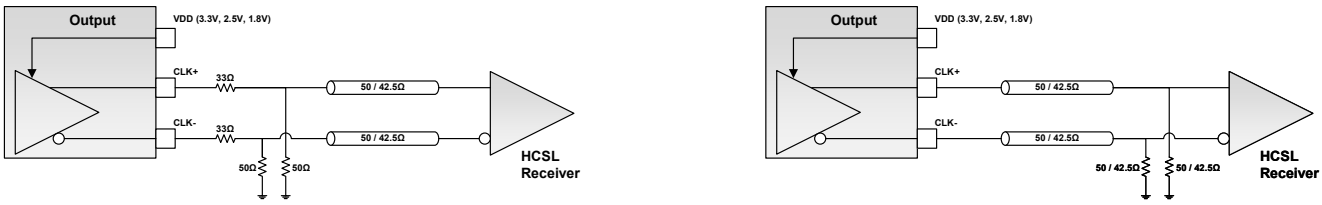
Figure 3.2. LVDS Output Terminations



AC-Coupled CML without VCM

AC-Coupled CML with VCM

Figure 3.3. CML Output Terminations



Source Terminated HCSL

Destination Terminated HCSL

Figure 3.4. HCSL Output Terminations

3.2. CMOS Output

Dual CMOS output format options support either complementary or in-phase signals for two identical frequency outputs. This feature enables replacement of multiple XOs with a single AS5004 device.

Figure 3.5. Integrated 1:2 CMOS Buffer Supports In-Phase or Complementary Outputs

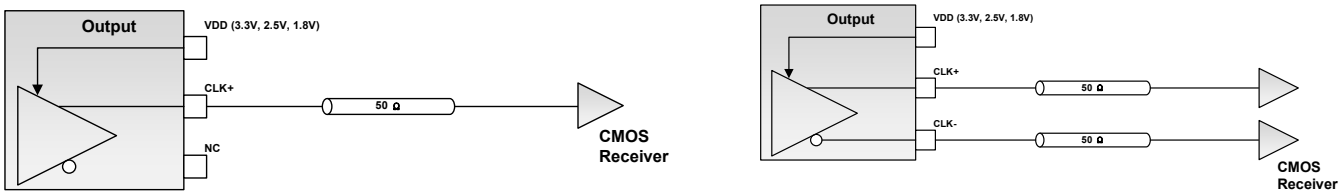


Figure 3.6. LVCMOS Output Terminations

4. Package Outline Drawing

Figure 4.1. shows the package outline drawing for the AS5004 devices. Details of dimensions for different size options are listed in Table 4.1. .

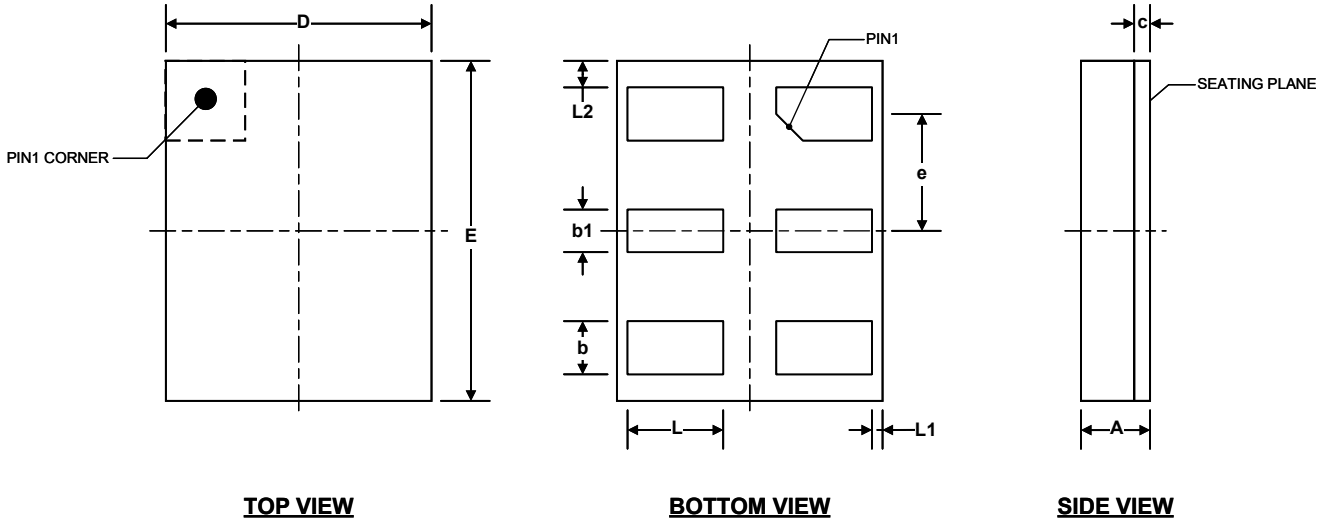


Figure 4.1. Package Outline Drawing

Table 4.1. Dimensions of Package Outline Drawing (mm)

Symbol	5032 Package	3225 Package	2520 Package
A	0.85 ± 0.05	0.85 ± 0.05	0.85 ± 0.05
b	0.64 ± 0.05	0.65 ± 0.05	0.55 ± 0.05
b1	0.64 ± 0.05	0.50 ± 0.05	0.40 ± 0.05
D	3.20 ± 0.10	2.50 ± 0.10	2.00 BSC
e	1.27 BSC	1.175 BSC	0.875 BSC
E	4.00 ± 0.10	3.20 ± 0.10	2.50 BSC
L	0.75 ± 0.05	0.70 ± 0.05	0.45 ± 0.05
L1	0.10 ± 0.05	0.10 ± 0.05	0.55 REF

5. Recommended PCB Land Pattern

Figure 5.1. shows the recommended PCB land pattern for the AS5004 devices. Details of dimensions for different size options are listed in Table 5.1. .

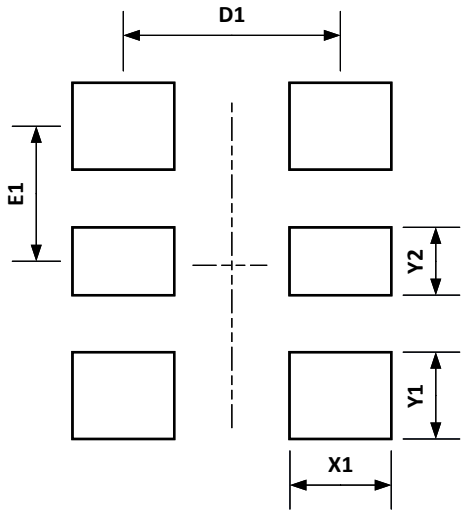


Figure 5.1. Recommended PCB Land Pattern

Table 5.1. Dimensions of Recommended PCB Land Pattern (mm)

Symbol	5032 Package	3225 Package	2520 Package
D1	2.35	1.70	1.00
E1	1.27	1.175	0.875
X1	1.05	1.00	0.75
Y1	0.84	0.85	0.75
Y2	0.84	0.70	0.60

Notes:

The following notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 um minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 0.8 1 for the pads.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6. Top Mark

Figure 6.1. shows the top mark specifications for the AS5004 devices. Description of each line is listed in Table 6.1.

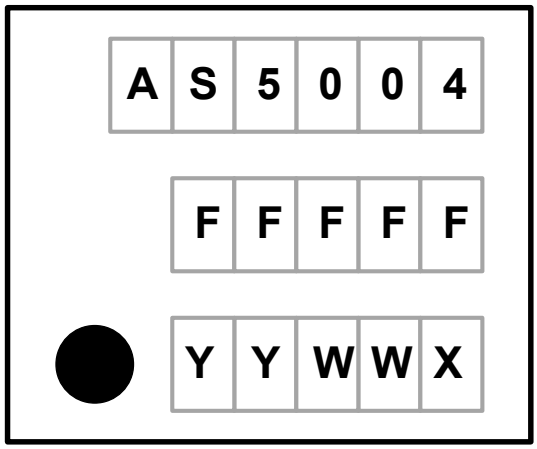


Figure 6.1. Top Mark

Table 6.1. Top Mark Description

Line	Position	Description
1	1-6	Device Name
2	1-5	Unique 5-digit Device Configuration Number
3	1	Pin 1 orientation mark (dot)
	2-3	Year (last two digits of the year), to be assigned by assembly site (ex: 2025 = 25)
	4-5	Calendar Work Week number (1-53), to be assigned by assembly site
	6	Manufacturer code

7. Packing Specification

Figure 7.1. shows the packing specifications for the AS5004 devices. Details of the tape specifications are listed in Table 7.1.
.

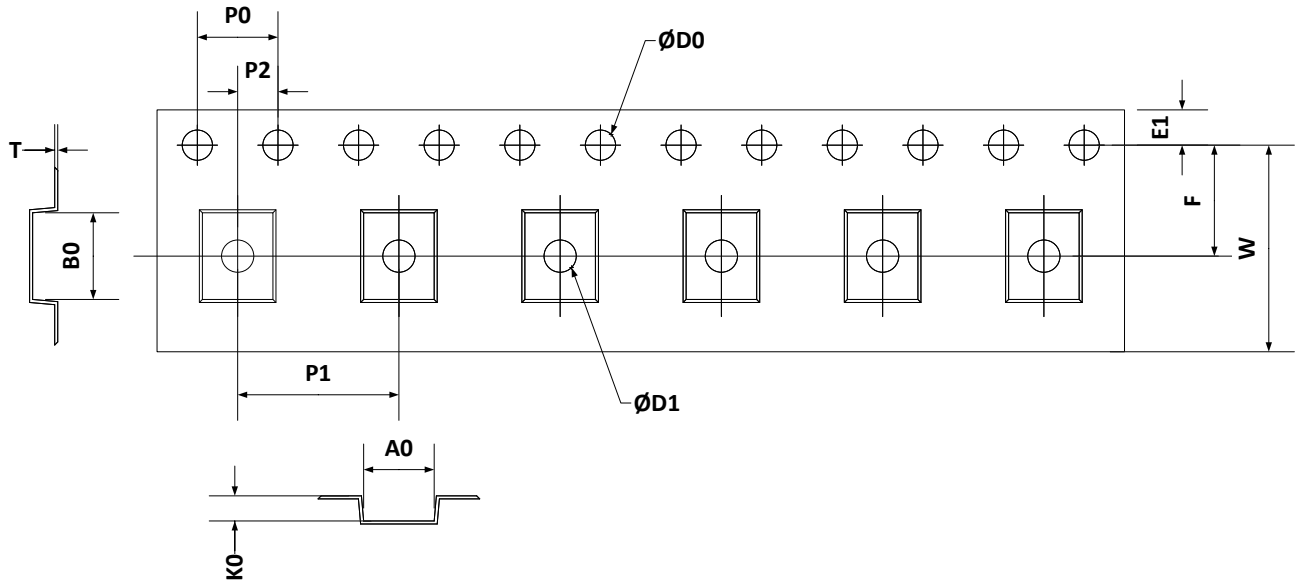


Figure 7.1. Tape Specification

Table 7.1. Dimensions of Tape (mm)

Symbol	5032 Package	3225 Package	2520 Package
A0	3.50 ± 0.10	2.80 ± 0.10	2.30 ± 0.10
B0	4.30 ± 0.10	3.50 ± 0.10	2.80 ± 0.10
K0	1.25 ± 0.10	1.05 ± 0.10	1.30 ± 0.10
E1	1.75 ± 0.10	1.75 ± 0.10	1.75 ± 0.10
F	5.50 ± 0.05	5.50 ± 0.05	5.50 ± 0.10
W	12.00 ± 0.30	12.00 ± 0.30	12.00 (+0.30/-0.10)
T	0.30 ± 0.05	0.30 ± 0.05	0.30 ± 0.05
P0	4.00 ± 0.10	4.00 ± 0.10	4.00 ± 0.10
P1	8.00 ± 0.10	8.00 ± 0.10	8.00 ± 0.10
P2	2.00 ± 0.05	2.00 ± 0.05	2.00 ± 0.10
ϕD0	1.50 ± 0.10	1.50 ± 0.10	1.50 (+0.10/-0)
ϕD1	1.60 ± 0.10	1.60 ± 0.10	1.05 ± 0.10

8. Important Notice and Disclaimer

Aeonsemi provides technical information such as datasheets, characterization reports, application notes, reference designs, and other resources “as is” and with all faults, and disclaims all warranties, express and implied, including without limitation any implied warranties of merchantability, fitness for a particular purpose or non-infringement of third-party intellectual property rights. These resources are subject to change without notice except when PCN is applicable. Aeonsemi grants you permission to use these resources only for development of an application that uses the Aeonsemi products described in the resource. Other reproduction and display of these resources are prohibited. No license is granted to any other Aeonsemi intellectual property right or to any third-party intellectual property right. Aeonsemi disclaims responsibility for, and you will fully indemnify Aeonsemi and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

Aeonsemi’s products are provided subject to Aeonsemi’s Terms of Sale (aeonsemi.com/terms) or other applicable terms available either on aeonsemi.com or provided in conjunction with such Aeonsemi products.

Contact: marketing@aeonsemi.com

9. Revision History

Revision	Date	Description
1.16	Oct 2026	Updated ordering guide
1.15	Aug 2026	Added 2520 package option Removed paragraph first-line indentation Corrected top mark position table
1.14	Jul 2026	Correct the LVPECL resistor value and the recommended PCB land pattern value
1.13	Aug 2025	Corrected the tape specification
1.12	Aug 2024	Add packing specification
1.11	Mar 2024	Updated the frequency offset
1.10	Jul 2022	Updated the top mark specification
1.01	Dec 2021	Adjusted the PCB land pattern dimensions
1.00	Sep 2021	With certain specification update
0.95	Jun 2021	Corrected the Ordering Guide Insert -40 - 105 ℃ temperature range option Insert section ”IMPORTANT NOTICE AND DISCLAIMER”
0.20	Mar 2021	Changed the frequency range and ordering guide
0.10	Feb 2021	Initial release