AS5019 Tiny Digital Controlled LVCMOS Silicon Oscillator

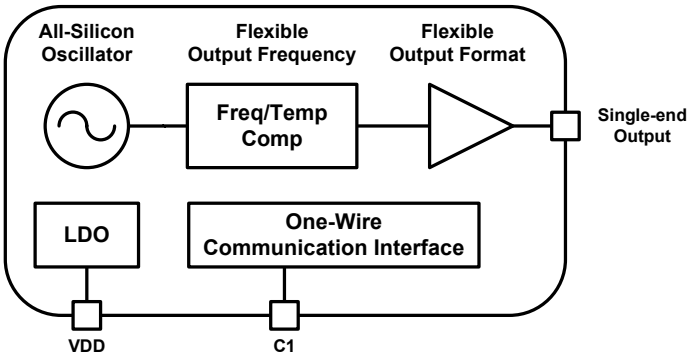
Description

The AS5019 all-silicon oscillator utilizes digital frequency synthesis and sensing technologies to provide a quartz-free, MEMS-free, low jitter clock at any output frequency. The device is factory-programmed to output frequencies ranging from 10 kHz to 125 MHz with 1 Hz resolution and maintains low jitter across its operating range.

There're no mechanical moving parts in the chip, which gives the AS5019 robust immunity to shock and vibration. The AS5019 uses on-chip temperature and strain sensors, and an advanced LC tank architecture to achieve excellent reliability even in high impact shock scenarios.

AS5019's on-chip power supply filtering provides ease of use in noisy systems with switched-mode power supplies.

The AS5019 is factory-configurable for a wide range of output frequencies. Specific configurations are factory programmed at time of shipment, eliminating the long lead times associated with custom oscillators. This process also guarantees 100% electrical testing of every device before shipment.



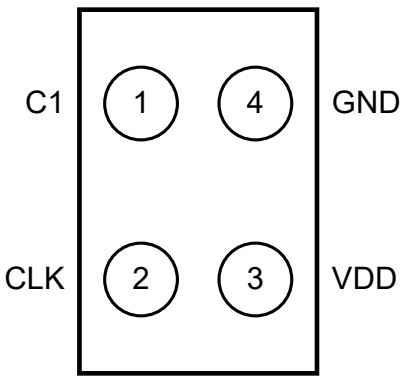
Key Features

- Quartz-free and MEMS-free without mechanical moving parts
- LVCMOS output: 10 kHz to 125 MHz
- Low jitter: 1 ps Typ
  (12 kHz – 20 MHz, @125 MHz)
- Operating temperature range:
  - -40 to 85 ℃ (Industial grade)
  - -40 to 105 ℃ (Extended-Industial grade)
- Frequency tolerance: ±50 ppm (-40 to 105 ℃)
- Immunity to shock and vibration
- Programmable output frequencies by one-wire communication interface
- Integrated LDO for on-chip power supply noise filtering
- Support 1.8V, 2.5V, 3.3V V_{DD} supply operation
- Tiny package size: 1.2 mm x 1.0 mm

Application

- IoT, Wearable device
- Health and medical monitoring
- Tablet
- Portable audio

Pin definition



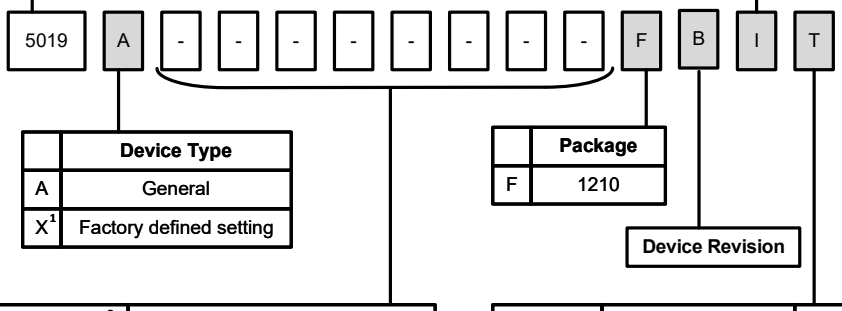
Top view

Pin#	Description
1	C1 = One-wire communication interface
2	CLK = Clock output
3	VDD = Power supply
4	GND = Ground

1. Ordering Guide

XO Series	Description
5019	Digital Control

	Device Grade	Temperature Grade
I	Industrial grade	-40 to 85°C
E	Extended Industrial grade	-40 to 105°C



	Device Type
A	General
X[1]	Factory defined setting

	Package
F	1210

Device Revision

Frequency Code[2]	Description
Mxxxxxxx	F_{CLK} < 1 MHz
xMxxxxxx	1 MHz <= F_{CLK} < 10 MHz
xxMxxxxx	10 MHz <= F_{CLK} < 100 MHz
xxxMxxxx	100 MHz <= F_{CLK} <= 125 MHz

Code	Packing type	Qty
T	7-inch reel	250
R	13-inch reel	2500
F	13-inch reel	5000
<blank>	ESD bag	Sample

Note:

1. “X” refers to the ID for the unique configuration with factory-defined settings, the value ranges from “B” to “Z”.
2. For example: 125 MHz = 125M0000; 33.33333 MHz = 33M33333.

2. Electrical Specifications

Table 2.1. Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
Operating Temperature Range						
Temperature Range	T_A	-40	–	85	℃	Industrial grade
		-40	–	105	℃	Extended industrial grade
Supply Voltage and Power Consumption						
Supply Voltage	V_{DD}	1.62	–	3.63	V	
Supply Current (F_{CLK} = 25 MHz)	I_{DD}	–	10	11	mA	Tristate Hi-Z (OE = 0)
		–	1	2	mA	Ready State (ACT = 0)
		–	12	14	mA	LVCMOS output (C_L=15pF)
Frequency Range						
Frequency Range	F_{CLK}	0.01	–	125	MHz	LVCMOS output
Frequency Tolerance						
Total frequency tolerance	F_{TOTAL}	-50	–	50	ppm	-40 - 105℃
Notes: Inclusive of initial frequency tolerance at 25℃, temperature stability over the corresponding operation temperature range, 10-year aging at 25℃ and variations over supply voltage, load and humidity after soldering-reflow shift settles.						
IO Characteristics						
One-Wire Comminication Interface(C1)	V_{IH}	0.7×V_{DD}	–	–	V	Input high voltage
	V_{IL}	–	–	0.3×V_{DD}	V	Input low voltage
	V_{OH}	0.83×V_{DD}	–	–	V	Output high voltage
	V_{OL}	–	–	0.17×V_{DD}	V	Output low voltage
Output Characteristics						
Powerup time	T_{OSC}	–	–	4	ms	Time from power reaches 0.9 × V_{DD} to output frequency (F_{CLK}) within spec
Duty cycle	DC	45	–	55	%	LVCMOS (C_L=15pF)
Rise/Fall time (20% to 80% VPP)	$T_{R/F}$	–	0.5	1.5	ns	LVCMOS (C_L=15pF)
LVCMOS	V_{OH}	0.83×V_{DD}	–	–	V	C_L=15pF
	V_{OL}	–	–	0.17×V_{DD}	V	
Phase Noise and Jitter						
RMS jitter BW: 12k - 20MHz	R_J	–	1	1.5	ps	F_{CLK} >= 100 MHz
		–	1.5	2	ps	F_{CLK} >= 25 MHz
Phase noise 125MHz LVCMOS output V_{DD} = 1.8 - 3.3V	PN_{1k}	–	-73	–	dBc/Hz	Phase noise at 1kHz offset
	PN_{10k}	–	-103	–	dBc/Hz	Phase noise at 10kHz offset
	PN_{100k}	–	-126	–	dBc/Hz	Phase noise at 100kHz offset
	PN_{1M}	–	-141	–	dBc/Hz	Phase noise at 1MHz offset
	PN_{10M}	–	-150	–	dBc/Hz	Phase noise at 10MHz offset

Continued on next page

Parameter	Symbol	Min	Typ	Max	Unit	Note
PSNR						
Spurs from power noise 50mV ripple V_{DD} = 1.8V	PSNR	–	-76	–	dBc	100 kHz sine wave
		–	-75	–	dBc	200 kHz sine wave
		–	-75	–	dBc	500 kHz sine wave
		–	-75	–	dBc	1 MHz sine wave
Spurs from power noise 50mV ripple V_{DD} = 2.5 or 3.3V	PSNR	–	-83	–	dBc	100 kHz sine wave
		–	-83	–	dBc	200 kHz sine wave
		–	-83	–	dBc	500 kHz sine wave
		–	-82	–	dBc	1 MHz sine wave

Table 2.2. Environmental Compliance and Package Information

Parameter	Value
Moisture sensitivity level (MSL)	3

Notes:

For additional product information not listed in the data sheet (e.g. RoHS Certifications, MSDS data, qualification data, REACH Declarations, ECCN codes, etc.), contact aeonsemi.com/contact_us

Table 2.3. Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Unit
Maximum operating temperature	T_{AMAX}	125	℃
Storage temperature	T_S	-55 - 125	℃
Supply voltage	V_{DD_MAX}	-0.5 - 3.8	V
Input voltage	V_{IN_MAX}	-0.5 - V_{DD}+0.3	V
ESD HBM (JESD22-A114)	HBM	4.0	kV
ESD CDM (JESD22-C101)	CDM	1.0	kV
Solder Temperature[2]	T_{PEAK}	260	℃
Solder time at T_{PEAK}[2]	T_P	20 - 40	sec

Notes:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

3. C1 Interface Overview

C1 is a single wire serial bidirectional interface for communication with the AS5019 device. It allows users to write/read registers in real time during application is running.

Summary of the features:

1. Single wire bidirectional byte oriented interface for writing and reading data bytes to and from the device.
2. Pulse width modulation (short pulse representing bit value 0, long pulse representing bit value 1) is used for data writes, level sensing is used for data bit reads.
3. The interface is byte oriented. Data is written and read in bytes.
4. There are 4 different C1 transactions with different transactions waveforms.
5. Each transaction is a separate C1 line waveform with transaction type and data embedded together into a single waveform.
6. Self-adjusting communication speed. Each individual C1 transaction can use different transfer speed.
7. Minimum speed limit. During data transfers C1 pulse must not be longer than 15 us.
8. Transaction self-reset capability. If the C1 transaction cannot be completed for whatever reason, the device internal hardware will reset the transaction processing if there is no level change on C1 line for 50 us.
9. C1 hardware implements digital deglitcher. All C1 pulses shorter than 50 ns are filtered out.
10. Each transaction can start at either low or high C1 line level.

Electrical requirements for external C1 master implementation:

1. Ability to drive C1 line with push-pull CMOS driver with low and high logical level, with low level being below 30% of V_{DD} and high level begin above 70% of V_{DD} where V_{DD} is the AS5019 device current power supply.
2. Ability to drive C1 line with variable width pulses. Different pulse width sequences implement different C1 transactions.
3. Ability to put the master C1 pin driver to high impedance state.
4. Ability to read back the value on the C1 line at some later time after the master C1 pin driver was put in high impedance state.

3.1. C1 Transaction Commands

Table 3.1. C1 Transaction Commands

Command	Data	Description
C1EAW	eaddr[15:0]	16 bit extended address write. Sets the address in C1 16 bit address register. Next C1DW data will be written to the 64 KB address space to this address.
C1EAW+	eaddr[15:0]	Like C1EAW, but sets internal autoincrement flag. Subsequent C1DW or C1DR will increment the 16 bit internal extended address after each successful C1DW data byte write or C1DR data byte read. Incremented internal C1 16 bit extended address saturates at 0xFFFF value.
C1DW	data[7:0]	Data byte write to currently set addr[7:0] address. Fast write without ready handshake.
C1DR	data[7:0]	Data byte read from currently set addr[7:0] address. Fast read without ready handshake.

If the address is set by **C1EAW**, the internal autoincrement flag is cleared and all subsequent **C1DW** and **C1DR** transactions data will be written to or read from the same address. The device internal address register does not change by data transactions.

If the address is set by **C1EAW+**, the internal auto increment flag setting is valid until their values are changed by the new **C1EAW** or **C1EAW+** transaction.

3.2. C1 Transaction Timing

Figure 3.1. shows **C1EAW** transaction timing as an example for the C1 transaction timing description.

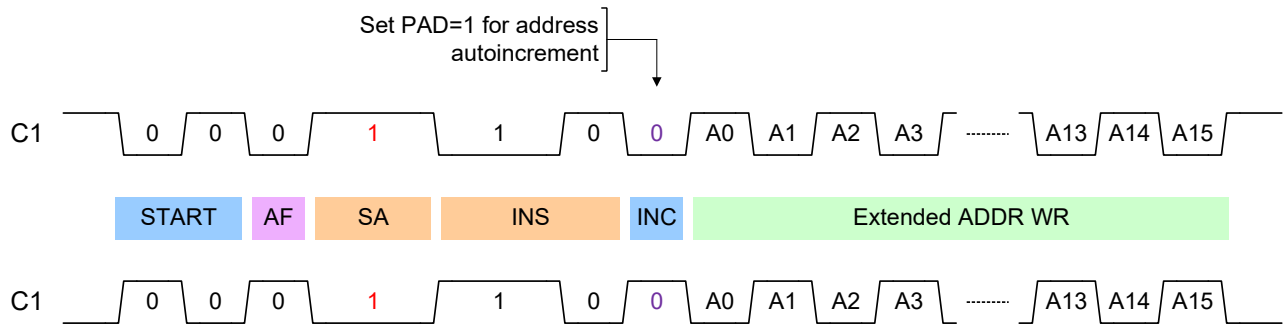


Figure 3.1. C1EAW (Extended Address Write) Transaction Timing

Each C1 transaction starts with the current C1 line level value. Since C1 transactions start and end at the same line level, they can start from either low or high level. That is why in this document all the waveforms are duplicated to show transactions starting at both high or low line level.

To switch the line level just change the C1 level and wait 50 us before starting next transaction.

From the current C1 level each transaction bit is represented by a short pulse of **Tzero** duration (bit value 0) or long pulse or **Tone** duration (bit value 1). The value 1 pulse **Tone** duration is usually recommended to be:

Tone >= 3 * **Tzero**

The transaction starts with two 0 bits in a row. Duration of those two bits (pulses) together is measured as a **Tstart** time and it is internally interpreted as 2 * **Tzero** time. After the first two pulses the subsequent pulse length **Tpulse** for each bit is measured and compared to the **Tstart** previously measured duration threshold.

If the pulse length is below **Tstart** threshold then it the pulse is considered representing bit value 0, when above the threshold then it is considered to be a bit value 1:

Tpulse < **Tstart** .. 0 bit

Tpulse >= **Tstart** .. 1 bit

This implies that the actual **Tzero** and **Tone** bit durations during the transaction do not have to be very precise since there is a **Tzero** time tolerance around the **Tstart** threshold for recognizing 0 or 1 bit. Therefore, the master pulse width time generation accuracy does not have to be very high since the device can tolerate quite a bit of pulse width “jitter” during the transaction.

First 7 bits of each transaction have fixed meaning described in the following table. Then address bits or data bits follow, always in little endian fashion, LSB data bit D0 or LSB address bit A0 being transferred first.

Table 3.2. C1 Transaction Fields

Field	Width[bits]	Description
START	2	**Start transaction** Two 0 bits (two Tzero pulses) back to back for transaction start.
AF	1	**Address Follows** For Aeonsemi factory use only. This bit must always be 0.
SA EXT	1	**Slow Access/Extended Address** Dual purpose bit based on transaction type. **SA .. Slow Access:** For Aeonsemi factory use only. **EXT .. Extended Address:** Set as 1 for C1EAW transaction.
INS	2	**Instruction type** Transaction (aka Instruction) encoding. The value of the bits determine the transaction type (bit on the left is sent first in time): 10 .. C1EAW (C1EAW, C1EAW+) 11 .. N/A (Aeonsemi factory use only) 00 .. C1DW 01 .. C1DR
PAD INC	1	**Pad/Auto increment** Dual purpose bit based on transaction type. **INC .. Auto increment:** For C1EAW transactions. If this bit is 1 then the transactions become C1EAW+. **PAD .. Padding:** For all other transactions. Dummy bit required to make odd number of transaction bits for the transaction to end at the same C1 line level as it started.

The limits of the C1 pulse durations and the key timing value of Tzero is in the following table.

Table 3.3. C1 Timing Parameters

Parameter	Min	Max	Description
Tzero	0.2 us	4 us	C1 bit value 0 duration and overall pacing time used for data reading timing as well. Measured in the device per transaction as **start** / 2
Tone	2.25 * Tzero	15 us	C1 bit value 1 duration
Tgap	max(1 us, 2 * Tzero)	—	Required time duration of steady C1 line in between two subsequent C1 transactions. The Tzero here is the duration of the bit 0 pulse or the previous transaction. By other words, the gap in between transactions is viewed a part of each transaction and is at each transaction's end.
Tread	max(4 us, Tone)	15 us	During of PAD pulse in C1DR transaction.
Treset	40 us	—	If C1 is steady without any level change for Treset time then the C1 internal transaction processing hardware will abandon the transaction and goes to its transaction processing ready state expecting the beginning of a new transaction.

The value of **Tzero** can change from transaction to transaction, but must stay constant during each transaction.

3.3. C1 Reset

During C1 transaction there must be C1 line level change at least every 20 us or less. This document mentions 15 us in all the timing tables, but the real hard value is 20 us. The 15 us mention is padded for reliable operation under all circumstances.

If the C1 line is without any changes for at least 40 us then the C1 current transaction processing (if any) is abandoned and the C1 internal hardware goes to its ready idle state expecting the beginning of the next transaction. Processing of any transaction can be abandoned at any time in the middle of it by keeping C1 line steady for 40 us or more.

4. C1 Address Write and Data Write Timing

4.1. C1 Address Write (C1EAW, C1EAW+)

Write the 16 bit address to the internal 16 bit address space address register. Note that if the bit **INC**=1 the transaction becomes **C1EAW+** transaction. Then the internal device 16 bit address will get incremented internally after each successfully finished **C1DW** or **C1DR** transaction. If the data transaction is aborted the internal address will not get incremented. For the autoincrement, the 16 bit extended address does not wrap around and saturates at 0xFFFF value.

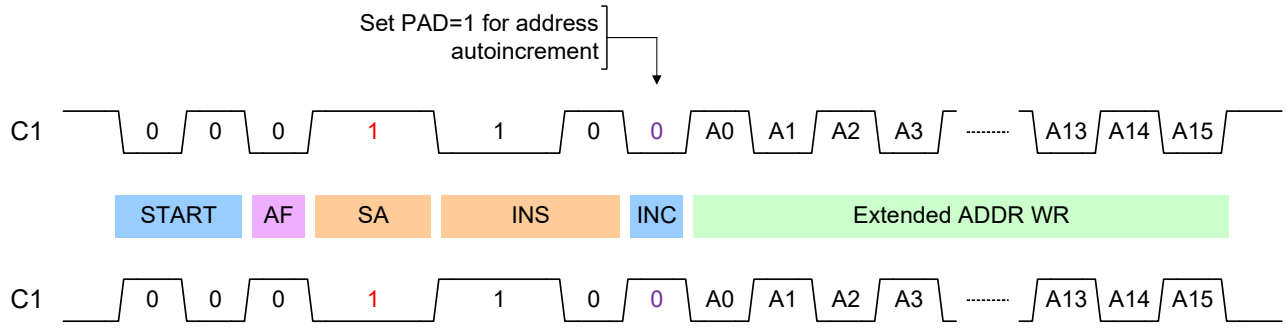


Figure 4.1. C1EAW[+] (Extended Address Write) Transaction Timing

4.2. C1 Data Write (C1DW)

Write data using internal fast data path invoked by the instruction encoding. For fastest timing keep the **PAD**=0 since the **PAD** bit value does not matter for **C1DW**. Note that the **C1DW** is the most used transaction and was designed to take shortest time possible.

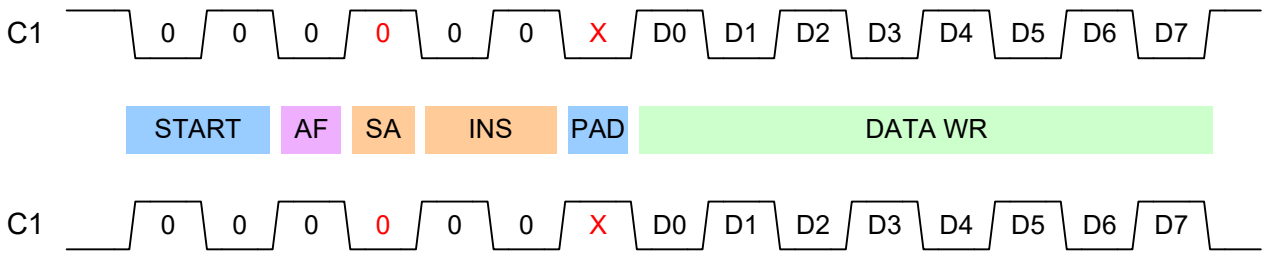


Figure 4.2. C1DW (Data Write) Transaction Timing

5. C1 Data Read Timing

Data byte needs to be read first internally in the device. The read data byte is then provided serially bit by bit to be read by the master using C1 line. During each bit read sequence the master is required to stop driving the C1 line at particular time and allow the device to drive the line by a single bit. Then the master reads the bit value and then starts driving the C1 line again to invoke another read bit sequence. The single bit read sequence needs to be repeated for all 8 data bits read from the device during each data read C1 transaction.

The read bits are provided in a little endian fashion, the LSB bit D0 of the read byte is provide first in time on the C1 line.

During the read sequence there is a weak internal level keeper with 3 kΩ resistor activated during the whole read bit sequence, starting after the **INS[1]** bit 1 is recognized and the internal read sequence is started as shown in Figure 5.3. The weak keeper keeps the last C1 level if both the internal device C1 driver and the C1 master external driver are both inactive in high impedance.

5.1. C1 Data Read (C1DR)

The Figure 5.1. below shows details about the **Fast C1RD** transaction timing using the fast read path invoked by the transaction encoding. The device internal byte read sequence is started the moment the second instruction bit **INS[1]**=1 level is recognized.

The duration of **PAD**=1 bits should be long enough for the device internal read to finish and provide the read data byte to the C1 hardware for the master to be able to read the read byte bit by bit in a serial fashion. The external master must extends the **PAD** bit duration to **Tread** time if the transaction **Tone** time would be too short. The recommended minimum time of **Tread** is 4 us.

The red parts of the read transaction waveforms mean that the C1 pin is driven by the device, not by the C1 master.

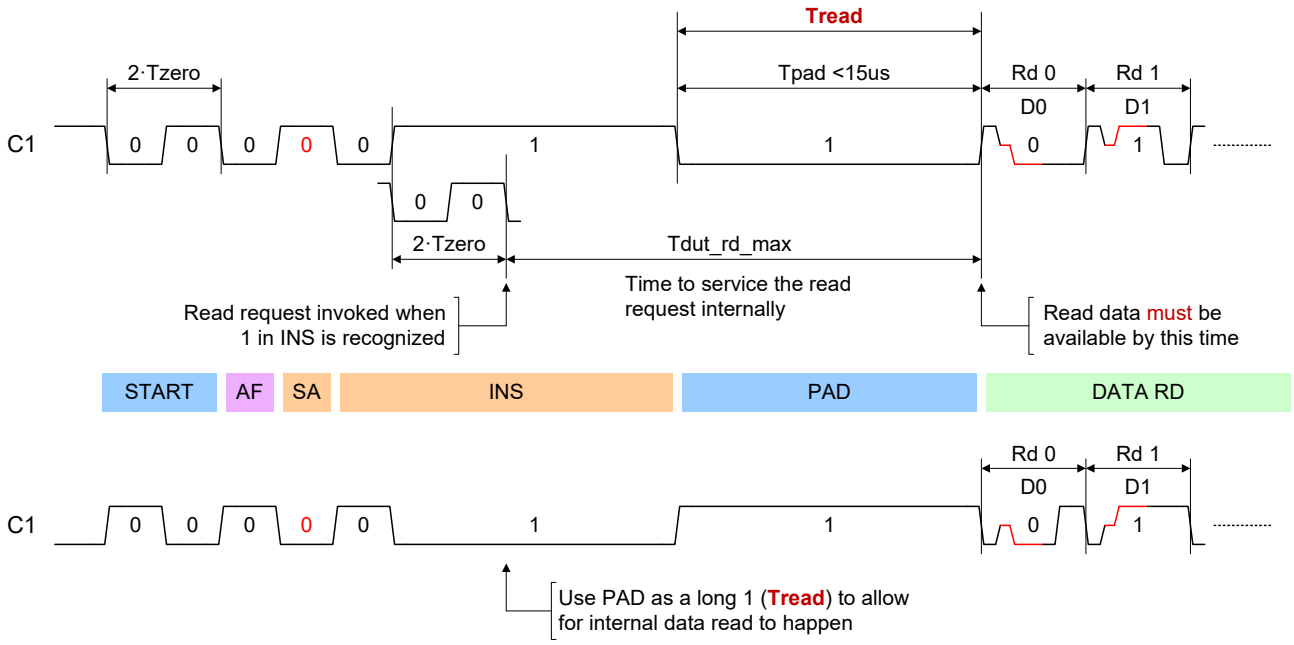


Figure 5.1. C1DR (Data Read) Transaction Timing Details

The full **C1DR** transaction timing for all read data bits is Figure 5.2.

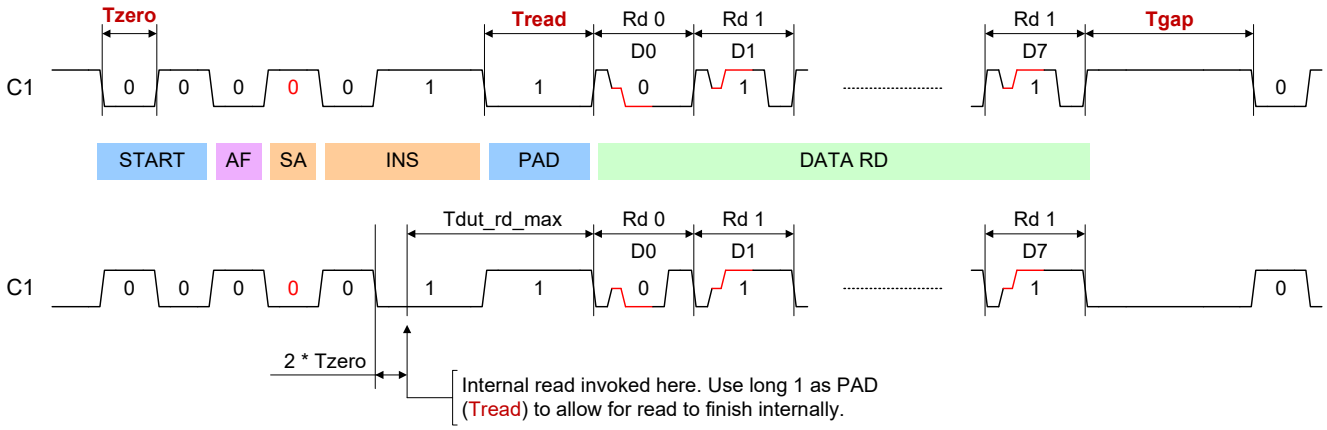


Figure 5.2. C1DR (Data Read) Full Transaction Timing

5.2. C1 Read Bit Timing

Data are read serially bit by bit. During each bit transaction the master is required to stop driving the C1 line at particular time and allow the device to drive the line for **Tzero** time. Then the master reads the bit value and then starts driving the C1 line again. The single bit read sequence needs to be repeated for all 8 data bits read from the device during each data read C1 transaction.

The details of the single read bit recommended implementation timing are in Figure 5.3.

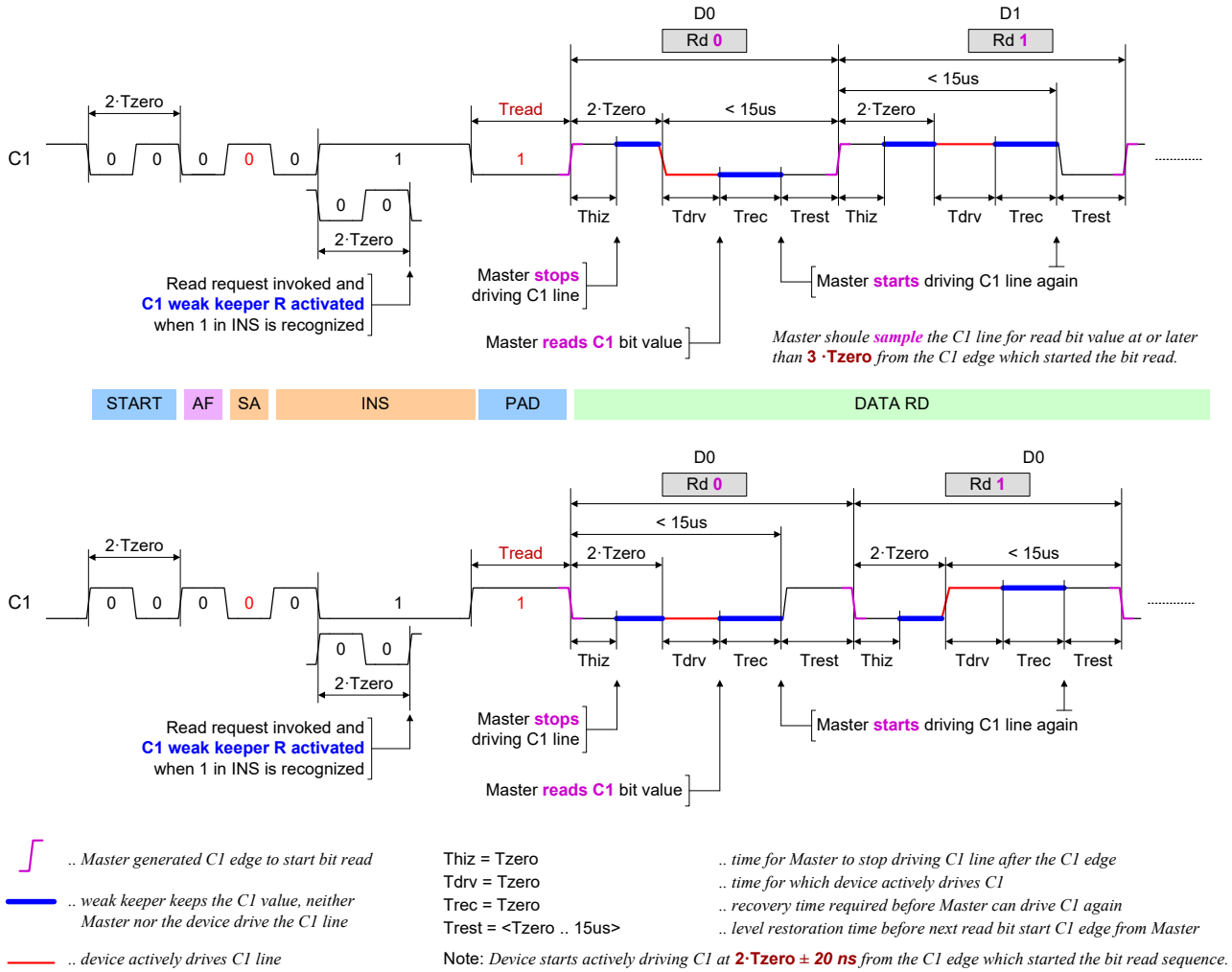


Figure 5.3. Recommended C1 Read Transaction Bit Read Timing

Each single bit read sequence is started by a C1 line value change edge. The first data read bit sequence is always started by the edge which ends the **PAD** pulse. The polarity of that edge is determined by the original C1 level at the beginning of the transaction. The same C1 edge polarity change then triggers the subsequent bit reads:

- C1 transaction starting level 1 .. all read bit sequences start by **rising** C1 edge
- C1 transaction starting level 0 .. all read bit sequences start by **falling** C1 edge

The recommended C1 master read bit sequence which needs to be issued 8 times back to back to read the whole data byte in its entirety is as follows:

1. While as master actively driving C1 line generate a bit read starting edge. The edge is determined by the C1 level at the beginning of the transaction as described above.
2. Wait **Tzero** time.
3. Stop driving the C1 line, putting the master C1 push pull driver to high impedance state.
4. Wait 2 * **Tzero** time.
5. Read the level value on C1 line. The read value is the value of the read data bit. Store it.
6. Wait **Tzero** time.
7. Start actively driving C1 with value which is the opposite the C1 level value at which the transaction started.
8. Wait **Tzero** time.
9. If not all bits have been read yet, go back to step 1. to generate another read bit sequence. If the last bit was just read, generate the same edge as in step 1. That puts the C1 line to the original level and marks the end of the transaction.
10. Wait **Tgap** time.
11. The device is ready to accept next transaction.

Each single bit read sequence takes 5 * **Tzero** time.

5.3. Detailed Read Bit Timing

This section is for reference and possibly debugging purposes only. The Figure 5.4. shows the actual exact timing for bit reading with timing tolerances of all the timing values. The figure served as a template to generate the recommended implementation setting described in Figure 5.3. above.

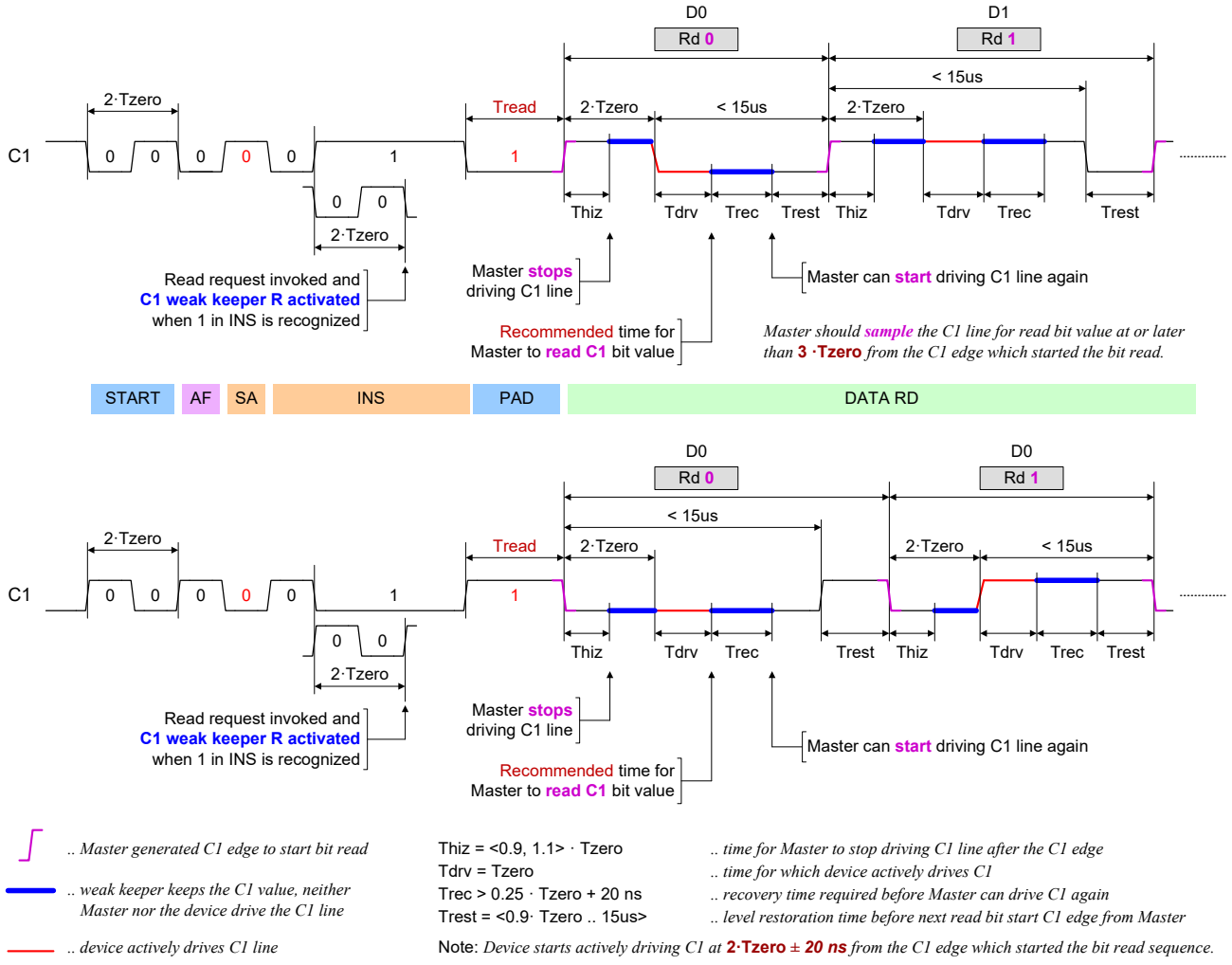


Figure 5.4. Detailed C1 Read Transaction Bit Read Timing

6. Configuring via C1 Interface

6.1. Device Operation

After an initial power up sequence, the device operates in either Ready state or an Active state depending on customization in factory. The Ready state is a power down standby state when majority of internal circuitries are powered down. The Active state is the device active mode with all internal circuitries powered up. Writing to register bUSYS_CTRL can move the device between Ready state and Active state.

The following three power up options are available for factory configuration:

1. Ready state: The device is in the power down standby mode. Writing transaction to register bUSYS_CTRL is required to enable the device and enable the Active state.
2. Active state with bODIV_CTRL=0: The device generates frequency internally, but output is disabled. Writing transaction to register bODIV_CTRL is required to enable output driver to propagate output frequency.
3. Active state with bODIV_CTRL=1: The device is fully functional, and output is enabled.

In the state 1 and 2 above, user can write to C1 to change drive mode or central frequency from the factory set values prior to enabling the device output or before moving to Active state.

6.2. Changing Frequency and Output Driver Mode

After startup, the device is at the factory set frequency, output driver strength, and device state. The device is ready to be controlled by C1 register writes. All register writes can take immediate effect, except fUSER_FREQ registers which require a follow on Apply command. User frequency register, “fUSER_FREQ”, is a 4-byte big endian register representing frequency as a binary32 IEEE 754-2008 standard number, in [Hz] units.

Changing frequency and driver mode requires two steps:

1. Writing fUSER_FREQ registers with the new desired central frequency and/or driver mode. Only the changing register needs to be written. Writing order in bytes is not essential. Writing these registers only records the new values, but does not invoke any internal processing.
2. Writing bUSYS_CTRL register with one of four Apply* commands. Once the Apply* command is accepted, the device uses the fUSER_FREQ register values and invokes internal central frequency and/or driver mode.

Changing frequency can be completed by either disabling the output driver or keeping the output drive enabled. This is determined by applying different Apply* commands. The bUSYS_CTRL values and descriptions are shown in Table 6.1.

Table 6.1. System Control Register bUSYS_CTRL

Value	Mnemonic	Description	stat_busy
0	UsysNop	No operation	—
1	UsysReady	Ready standby power down state	—
2	UsysActive	Active state	—
3	reserved	No operation	—
4	UsysRstSys	Invoke system reset restart	—
5	UsysRstPor	Invoke power-on reset restart	—
6	reserved	Do not use	—
7	reserved	Do not use	—
8	UsysApply	Apply: Disable output if active, update only changed frequency/driver mode	Check/Set
9	UsysApplyForce	Apply force: Disable output if active, force frequency/driver mode update	Check/Set
10	UsysApplyAct	Apply active: Keep output running if active, update only changed frequency/driver mode	Check/Set
11	UsysApplyActForce	Apply active force: Keep output running if active, force frequency/driver mode update	Check/Set
12	UsysRefresh	Refresh: Refresh fUSER_FREQ and bDRV_MODE register values to reflect the actual current device frequency and driver mode settings	Check/Set
Others	UsysNop	Do not use	—

Writing to “bUSYS_CTRL” register generates an acceptance request. When this command is accepted, the “bUSYS_CTRL” register is cleared. If a read from “bUSYS_CTRL” returns a non-zero value, it means that the writing command is still waiting to be accepted. A command acceptance happens in less than 5 us from the finishing of writing to the “bUSYS_CTRL” register. An accepted command can be either processed or ignored.

Commands other than “Apply*” and “Refresh” are always processed after the acceptance. It is possible to interrupt any “Apply*” or “Refresh” command under processing. A processing time depends on the command and its current state of the device, in most cases it is from 1 to 5 us, but can be up to 160 us when the command is generated in the middle of the frequency change.

“Apply*” and “Refresh” commands are only processed when “bUSYS_STATS.stat_busy” = 0. When “bUSYS_STATS.stat_busy” = 1, although new “Apply*” and “Refresh” commands are accepted, they are ignored. The “bUSYS_STATS.stat_busy” = 1 status bit is the beginning of internal processing. The “bUSYS_STATS.stat_busy” = 0 occurs after this internal processing finishes. Changing frequency and output driver must be completed before invoking a new command.

Issuing a “Refresh” command reset the values of registers to match the actual state of the device. During a normal operation, the device keeps the values of fUSER_FREQ synchronized with the internal state of the device. Reading these registers represent the actual frequency and output driver mode. However, the values could be different if writing occurs before applying the “Apply*” or “Refresh” command. If the “Apply*” command is not applied, then the registers value are the previous written values. Thus, issuing the “Refresh” command is necessary.

“fUSER_FREQ” and “bUSYS_STAT” registers are located back to back in C1 address space. As a result, the most used operation is done in C1 transaction as shown below. This example shows changing the frequency to a 70 MHz, which corresponds a 32-bit floating point number, 0x4c8583b0 in [Hz]. It is followed by a **“Apply”** command to invoke the internal frequency update, and assumed that the C1 register address auto increment is enabled, which is a default.

Example of programming to 70 MHz:

1. C1EAW+ 0x4055 — Address starts from 0x55, the first byte of “fUSER_FREQ”
2. C1DW 0x4C — Starts writing data to “fUSER_FREQ”
3. C1DW 0x85
4. C1DW 0x83
5. C1DW 0xB0 — Last byte write of “fUSER_FREQ”
6. C1DW 0x08 — Write data to “bUSYS_STAT”

6.3. System Status

“bUSYS_STAT” is a read only system status register. It is readable any time and it reflects the current device status. All possible values of the register are listed in Table 6.2.

Table 6.2. System Status bUSYS_STAT Register Values

bUSYS_STAT								Description
stat_busy			stat_trans	stat_rst	stat_tune	stat_active	stat_ready	
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
0	0	0	0	0	0	0	0	Start up
v	0	0	0	0	0	0	1	Ready state
v	0	0	0	0	0	1	0	Active state
v	0	0	0	0	1	1	0	Active state, tuning to new frequency
v	0	0	1	0	0	0	1	Ready to Active transition
v	0	0	1	0	0	1	0	Active to Ready transition
0	0	0	1	1	0	0	0	Reset processing, shutting down
0	0	0	0	1	0	0	0	Reset accepted

stat_busy bit [7] value v denotes value 0 or 1. The bit is 1 at the beginning of Apply* and Refresh commands internal processing and is 0 when the processing is done.

6.4. Center Frequency Control

Changing “fUSER_FREQ” register value controls the center frequency. The step does not apply to the DCXO feature. Frequency change request shown in Figure 6.1. and Figure 6.2.

Figure 6.1. shows a timing of frequency change by using “Apply” command when a “fUSER_FREQ” register value is different from the current frequency; or using “ApplyForce” command with the output disabled during the frequency change.

Figure 6.2. marks the time when a “Apply*” command is written to a “bUSYS_CTRL” register which corresponds with the write of the last data bit to this “bUSYS_CTRL” register.

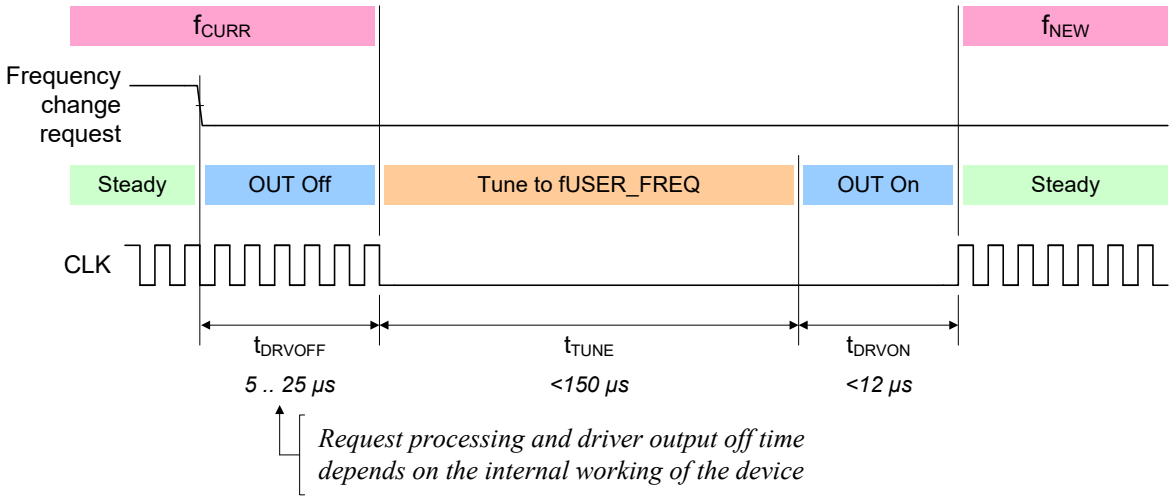


Figure 6.1. Frequency Change by “Apply” Command

Figure 6.2. shows either using an “ApplyAct” command when a “fUSER_FREQ” register has different value from the current frequency; or using an “ApplyActForce” command when the output keeps active during the frequency change. No signal glitches at the output occurs during the frequency change. However, there could be some periods in the output frequency corresponding when the current frequency and new frequency interval are not aligned. This behavior is device dependent and it also depends on the actual values and relationships in between the current and new frequencies.

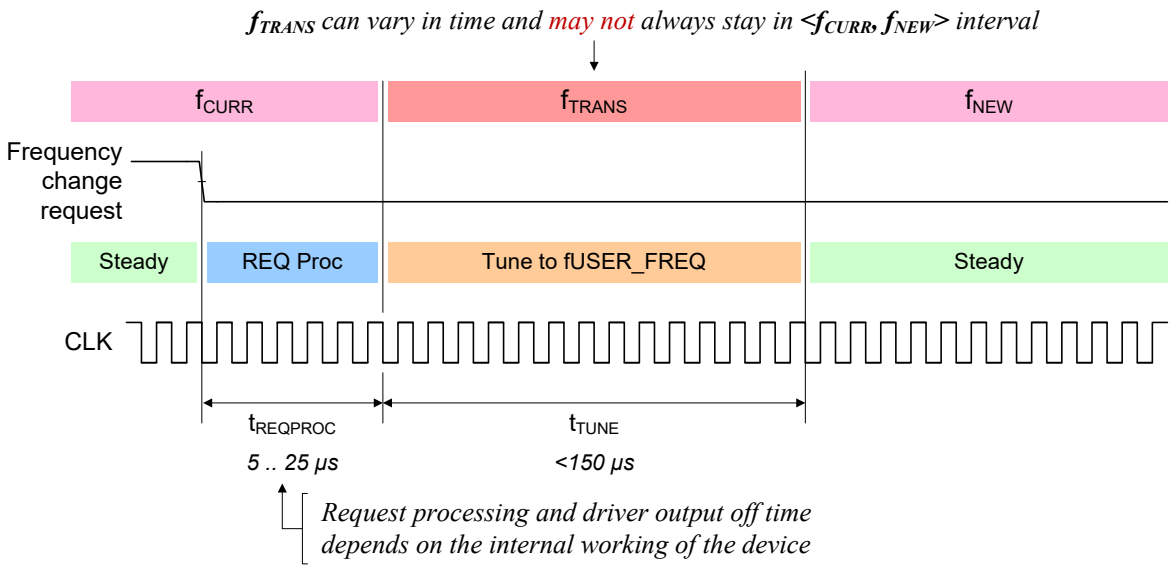


Figure 6.2. Frequency Change by “ApplyAct” Command

6.5. C1 Register Reference

The C1 interface is a byte-oriented interface. Registers are wider than 8 bits requiring to be split into multiple bytes located on subsequent register addresses. There are two types of multi byte registers:

1. Array of arrays, prefix ab, for example abUSER_ID[4] are organized in little endian fashion, byte abUSER_ID[0] is located at the lowest address, and the last byte of the array abUSER_ID[3] is located at the highest address.
2. An assigned 32-bit long integer, prefix j, and a 32-bit IEEE 754-2008 floating point number, prefix f are organized in big endian fashion, such that the most significant byte (MSB) is located at the lowest address.

Any unassigned byte registers have prefix b. Registers in the C1 address space 0x00...0xFF without specifications in the register description table are reserved for factory use. All register bit fields labeled [reserved] are read only and are reserved for factory use. Read value should be ignored. Any register bits not specifically mentioned in “Bits” columns are unused. Writing to these registers is ignored and a read always returns a 0. Numerical values are either hexadecimal with 0x prefix or decimal without any prefix.

Descriptions of register table columns:

Table 6.3. Register Table Columns

Register	Description
Addr	C1 register address.
Register	Register name.
Bytes	Number of bytes in the register. Wider than single byte registers span several subsequent bytes in an address space.
Endian	Endian for registers wider than one byte. Not applicable for single byte registers.
B	Big endian. The most significant byte (MSB) of the register appears at the lowest address.
L	Little endian. The least significant byte (LSB) of the register appears at the lowest address.
Field	Field name within the register.
[reserved]	Reserved for factory use and readable only
Bits	Field bit locations within a register. When the field spans more than one bit, the [M:L] notate. Denoting locations of a most significant bit M and a least significant bit L within the register are used.
Type	Field access type.
R/W	Read/write field by C1.
R	Read only field by C1.
W1	Writing a 1 triggers an associated event, while writing a 0 has no effect. A read always returns 0.
Rst	Field reset value. The value ‘Factory’ indicates that the value depends on the individual device factory configuration.

6.6. Register Map

Table 6.4. User Identification

Register	Addr	Field	Bits	Type	Rst	Description
abCFG_ID[6]	0x402d	cfg_id	[47:0]	R	Fact	Factory device configuration identification.

Table 6.5. User Output Divider Enable

Register	Addr	Field	Bits	Type	Rst	Description
bODIV_CTRL	0x403c	odiv_oe_ena	[0]	R/W	1	Output divider and driver output enable. 0 .. disable 1 .. enable
bPMUX_CFG0	0x4067	pmux_sel0	[2:0]	R/W	0	PMUX function 0 (ODIV OE == DRV OE) input GPIO select index. Value 7 changes Pin1 function from C1 communication to hardware controlled output enable.
		pmux_inv0	[7]	R/W	0	When set to 1 invert the active level of selected GPIO input making it active low.
bGPIO_DIN_ENA	0x406f	gpio_din_ena	[0]	R/W	0	Pin1 data input path enable. Need to be set together with the bPMUX_CFG0 configuration to turn on Pin1 hardware OE function.

Table 6.6. User System Control

Register	Addr	Field	Bits	Type	Rst	Description
fUSER_FREQ[4]	0x4055	user_freq	[31:0]	R/W	Fact	Floating point binary32 IEEE 754-2008 number in big endian representation with the most significant byte at the lowest address. It represents user desired output center frequency in [Hz]. C1 write to fUSER_FREQ has no immediate effect. The user is required to write a command to bUSYS_CTRL register to invoke the frequency change process.
bUSYS_CTRL	0x4059	usys_ctrl	[31:0]	R/W	Fact	User system control. Command byte to be written whenever the frequency change, driver mode change, or special system action is required. See Table 6.1. for command values.
bUSYS_STAT	0x405a	stat_ready	[0]	R	0	Ready state reached.
		stat_active	[1]	R	0	Active state reached.
		stat_tune	[2]	R	0	In Active tuning to a new frequency. If 1, then stat_active = 1.
		stat_rst	[3]	R	0	Reset request accepted.
		stat_tran	[4]	R	0	In system state transition. Based on the initial state the device is transitioning from, bUSYS_STAT.stat_ready, bUSYS_STAT.stat_active, or bUSYS_STAT.stat_rst is set to 1.
		stat_busy	[7]	R	0	Busy processing tuning to a new frequency and/or driver mode change. This bit is checked, set, and cleared only by Apply* and Refresh commands.

7. Package Outline Drawing

Figure 7.1. shows the package outline drawing for the AS5019 devices. Details of dimension for different size options are listed in Table 7.1.

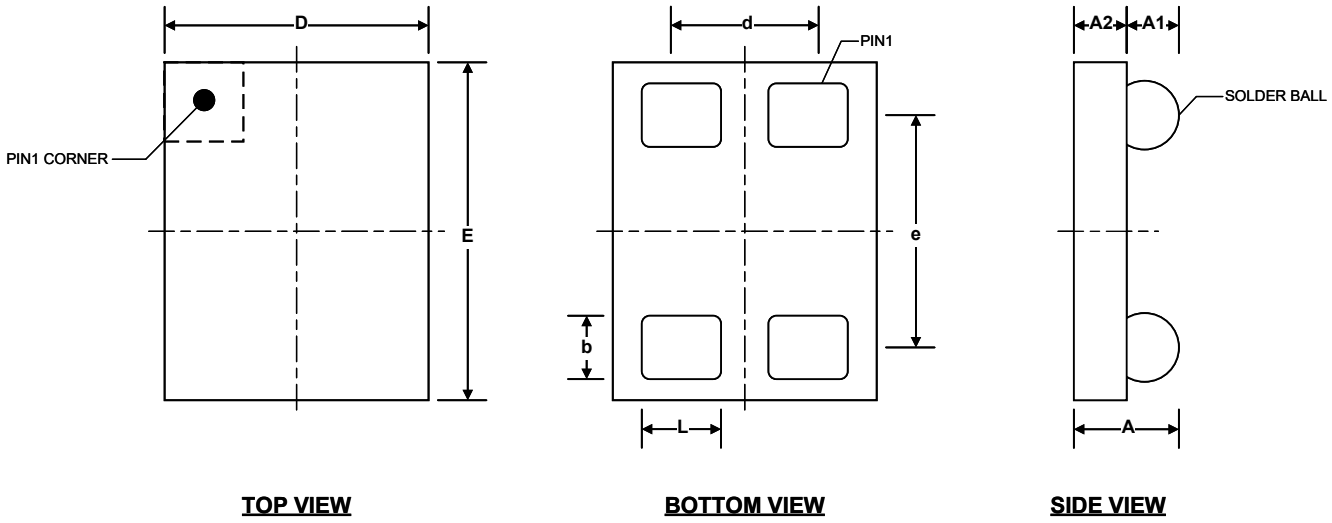


Figure 7.1. Package Outline Drawing

Table 7.1. Dimensions of Package Outline Drawing (um)

Symbol	Min	Nom	Max
A	505	540	575
A1	120	130	140
A2	385	410	435
b	225	235	245
d	–	410 BSC	–
D	1027.2	1052.2	1077.2
d	–	958.2 BSC	–
E	1243.2	1268.2	1293.2
L	250	260	270

8. Recommended PCB Land Pattern

Figure 8.1. shows the drawing of recommended PCB land pattern for the AS5019 devices. Details of dimension for different size options are listed in Table 8.1.

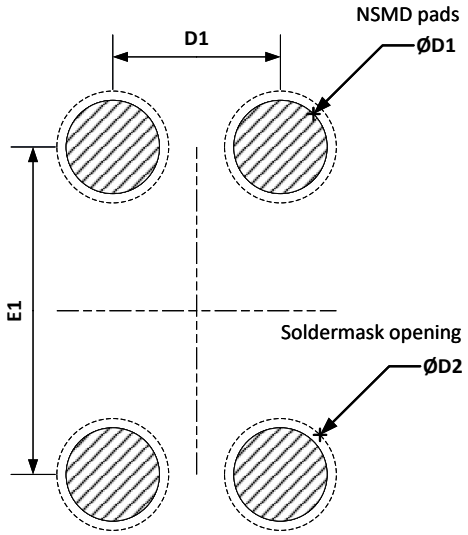


Figure 8.1. Recommended PCB Land Pattern

Table 8.1. Dimensions of Recommended PCB Land Pattern (mm)

Symbol	1210 Package
D1	0.41
ØD1	0.25
ØD2	0.35
E1	1.00

Notes:

The following notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 0.8 1 for the pads.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Top Mark

Figure 9.1. shows the top mark specifications for the AS5019 devices. Description of each line is listed in Table 9.1.

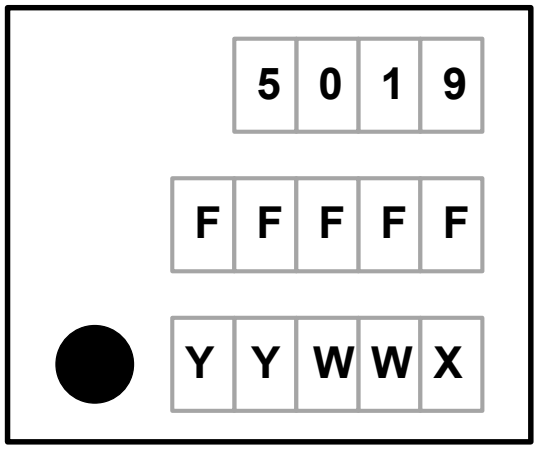


Figure 9.1. Top Mark

Table 9.1. Top Mark Description

Line	Position	Description
1	1-4	Device Name
2	1-5	Unique 5-digit Device Configuration Number
3	1	Pin 1 orientation mark (dot)
	2-3	Year (last two digits of the year), to be assigned by assembly site (ex: 2025 = 25)
	4-5	Calendar Work Week number (1-53), to be assigned by assembly site
	6	Manufacturer code

10. Packing Specification

Figure 10.1. shows the packing specifications for the AS5019 devices. Details of the tape specifications are listed in Table 10.1. .

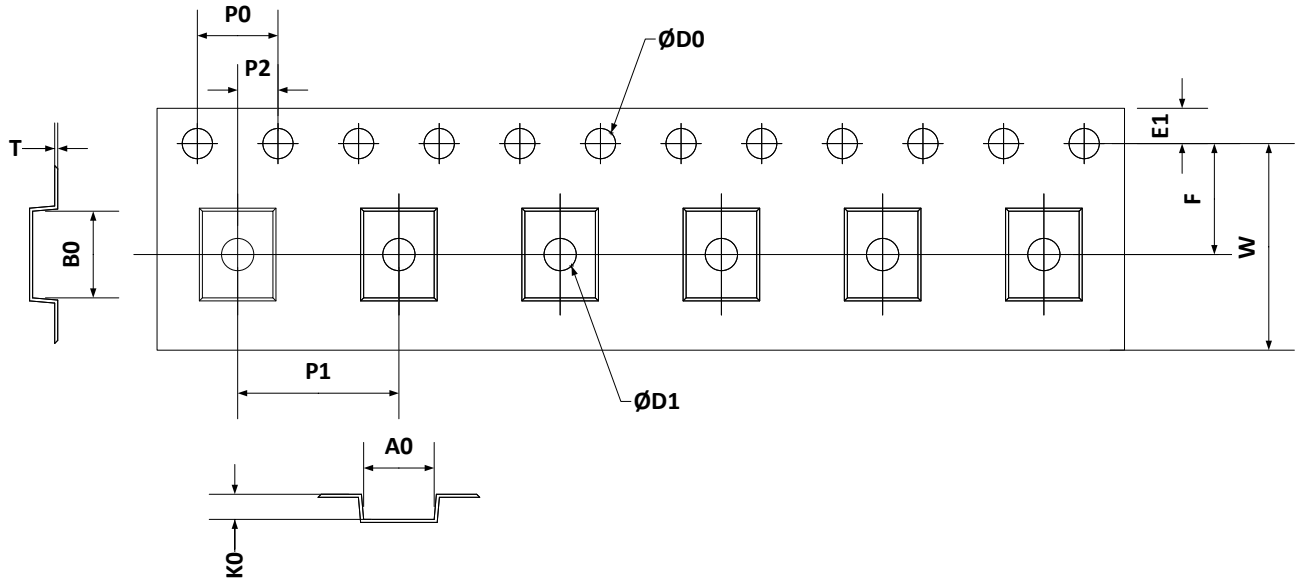


Figure 10.1. Tape Specification

Table 10.1. Dimensions of Tape (mm)

Symbol	1210 Package
A0	1.20 ± 0.03
B0	1.42 ± 0.03
K0	0.63 ± 0.03
E1	1.75 ± 0.10
F	3.50 ± 0.05
W	8.00 (+0.30/-0.10)
T	0.20 ± 0.02
P0	4.00 ± 0.10
P1	4.00 ± 0.10
P2	2.00 ± 0.05
ϕD0	1.55 ± 0.05
ϕD1	0.60 ± 0.05

11. Important Notice and Disclaimer

Aeonsemi provides technical information such as datasheets, characterization reports, application notes, reference designs, and other resources “as is” and with all faults, and disclaims all warranties, express and implied, including without limitation any implied warranties of merchantability, fitness for a particular purpose or non-infringement of third-party intellectual property rights. These resources are subject to change without notice except when PCN is applicable. Aeonsemi grants you permission to use these resources only for development of an application that uses the Aeonsemi products described in the resource. Other reproduction and display of these resources are prohibited. No license is granted to any other Aeonsemi intellectual property right or to any third-party intellectual property right. Aeonsemi disclaims responsibility for, and you will fully indemnify Aeonsemi and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

Aeonsemi’s products are provided subject to Aeonsemi’s Terms of Sale (aeonsemi.com/terms) or other applicable terms available either on aeonsemi.com or provided in conjunction with such Aeonsemi products.

Contact: marketing@aeonsemi.com

12. Revision History

Revision	Date	Description
1.02	Oct 2026	Updated ordering guide
1.01	Oct 2026	Updated several items
0.10	Sep 2025	Corrected several description errors
0.09	Aug 2025	Update the package outline
0.08	May 2024	Correct several mistakes
0.07	Feb 2024	Update the initial tolerance and temperature stability
0.06	Sep 2023	Update the initial tolerance
0.05	Jul 2023	Update the top mark and ordering guide
0.04	Jun 2023	Correct C1AW transaction to C1EAW
0.03	Jun 2023	Add C1 data programming interface protocol
0.02	May 2023	Updated the core power consumption
0.01	Nov 2022	Initial release