

## AS5223 Ultra Low Jitter Low Power I<sup>2</sup>C Programmable Differential DCTCXO

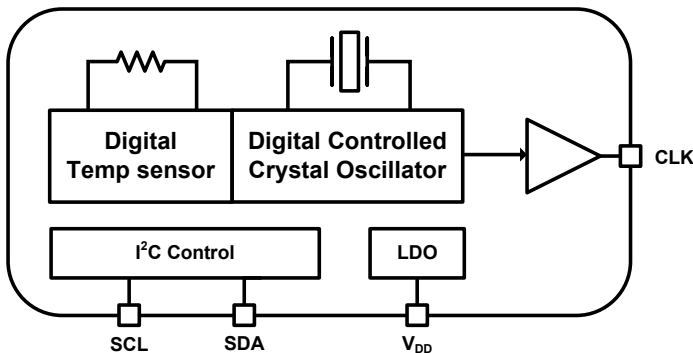
### Description

The AS5223 is a digitally controlled temperature compensated crystal oscillator (DCTCXO) with a pair of low-amplitude LVCMOS output clock between 10 MHz and 156.25 MHz. The AS5223 utilizes digital temperature sensing and frequency compensation technologies to provide a high precision, temperature stabilized clock with grade options from  $\pm 5$ ppm to  $\pm 20$ ppm.

The AS5223 operates in a wide power supply range from 1.5V to 3.3V. The on-chip LDOs ensure robust power supply noise rejection which simplifies the external supply noise filtering requirements.

The AS5223 supports configurable output amplitude from 0.8V to 1.2V. The 0.8V output option is compliant with clipped sine (0.8V CS) which is widely adopted in the industry. The two outputs can be configured as in-phase or complementary. When it's configured as complementary, the outputs can be used as a differential pair.

Available in industry-standard 2016 package, the AS5223 comes in industrial, extended industrial and automotive device grades. Specific combination of package, frequency, stability, driver format, and device grade can be selected at the time of ordering.



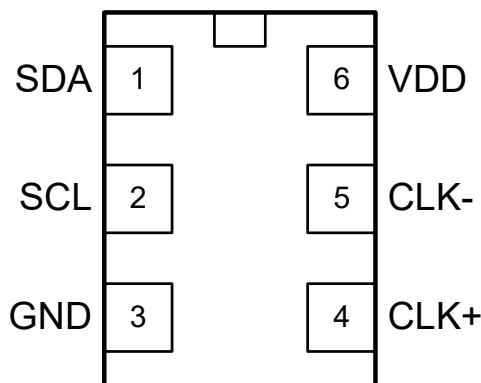
### Key Features

- Frequency range: 10 to 156.25 MHz
- Dual LVCMOS and Differential output options
- 0.8, 1.0, 1.2V output amplitude/swing options
- Ultra-low jitter: 52 fs Typ (12 kHz – 20 MHz, @156.25 MHz)
- Ultra-low core power: 5mA
- Operating temperature range:
  - -40 to 85 °C (Industrial grade)
  - -40 to 105 °C (Extended-Industrial grade)
  - -40 to 105 °C (AEC-Q100 grade 2)
- Temperature stability:
  - $\pm 5$  ppm (Grade S)
  - $\pm 20$  ppm (Grade D)
- Programmable output frequencies and formats by I<sup>2</sup>C communication interface
- Integrated LDO for on-chip power supply noise filtering
- 1.5V to 3.3V V<sub>DD</sub> supply operation
- Standard DFN 2016 package

### Application

- Microwave backhaul
- Communication networks
- Data center interconnect
- AI server clusters
- Smart network interface card
- High-speed optical module

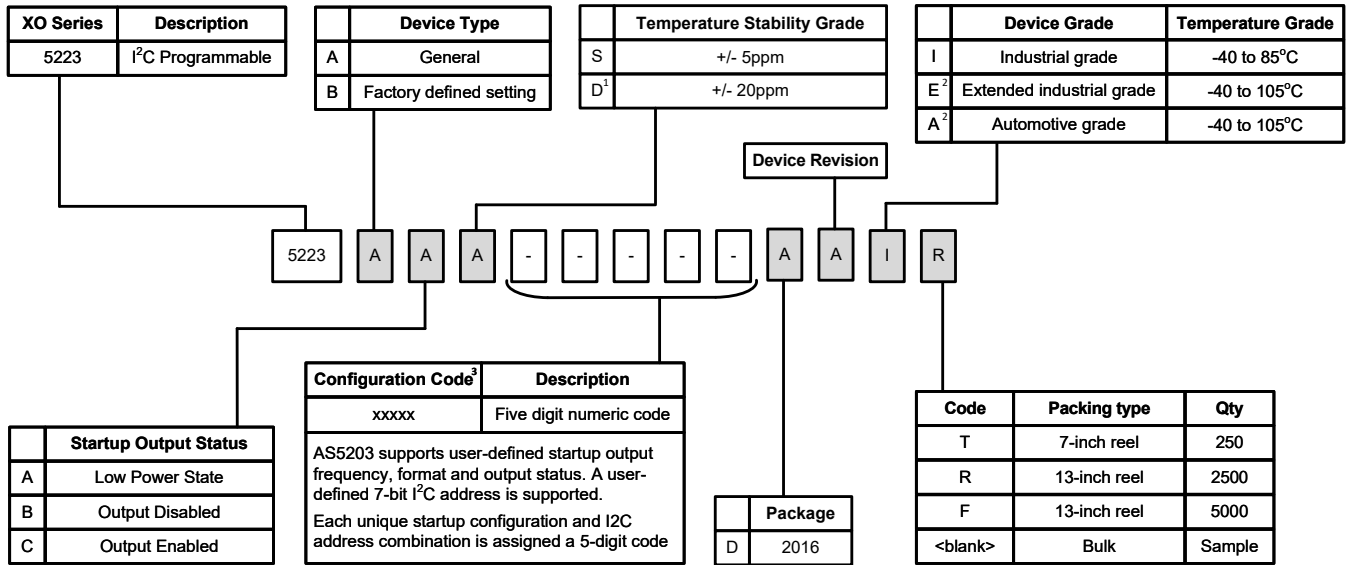
### Pin definition



Top view

| Pin# | Description                         |
|------|-------------------------------------|
| 1    | SDA = I <sup>2</sup> C serial data  |
| 2    | SCL = I <sup>2</sup> C serial clock |
| 3    | GND = Ground                        |
| 4    | CLK+ = Clock output                 |
| 5    | CLK- = Complementary clock output   |
| 6    | VDD = Power supply                  |

## 1. Ordering Guide



### Note:

1. Temperature compensation is not applied for grade-D device. Frequency is calibrated at 25 °C in production test.
2. Contact Aeonsemi for “Extended industrial” and “Automotive” grade device.
3. The five-digit numeric code is an identification of the configurations. Check the datasheet appendix for the details.

## 2. Electrical Specifications

Table 2.1. Electrical Specifications

| Parameter  | Symbol             | Min   | Typ | Max                  | Unit  | Note   |
|--|--------------------|---|-----|----------------------|-------|--|
| Operating Temperature Range  |                    |   |     |                      |       |  |
| Temperature Range  | T <sub>A</sub>     | -40   | —   | 85                   | °C    | Industrial grade   |
|  |                    | -40   | —   | 105                  | °C    | Extended industrial grade  |
|  |                    | -40   | —   | 105                  | °C    | Automotive AEC-Q100 Grade2   |
| Supply Voltage and Power Consumption   |                    |   |     |                      |       |  |
| Supply Voltage   | V <sub>DD</sub>    | 1.425   | —   | 3.63                 | V     | Core voltage   |
| Driver Regulator Voltage   | V <sub>R</sub>     | 0.8   | —   | 1.2                  | V     | Regulator voltage  |
| Supply Current<br>(F <sub>CLK</sub> = 156.25 MHz)  | I <sub>CORE</sub>  | —   | 4   | 5                    | mA    | Tristate Hi-Z (Output disabled)  |
|  | I <sub>DRV</sub>   | —   | 1.6 | 2                    | mA    | 0.8V LVCMOS (Load = 10pF // 10kΩ)  |
|  |                    | —   | 2   | 2.5                  | mA    | 1.0V LVCMOS (Load = 10pF // 10kΩ)  |
|  |                    | —   | 2.4 | 3                    | mA    | 1.2V LVCMOS (Load = 10pF // 10kΩ)  |
|  |                    | —   | 6   | 7                    | mA    | 0.8V Differential (100 Ω termination)                                      |
|  |                    | —   | 7.5 | 9                    | mA    | 1.0V Differential (100 Ω termination)                                      |
|  |                    | —   | 9   | 11                   | mA    | 1.2V Differential (100 Ω termination)                                      |
| Frequency Range  |                    |   |     |                      |       |  |
| Frequency Range  | F <sub>CLK</sub>   | 10  | —   | 156.25               | MHz   | Standard frequency options<br>Contact Aeonsemi for other frequency options |
|  |                    | 10, 16, 19.2, 20, 25, 26, 32, 38.4, 50, 52, 100, 155.52, 156.25 |     |                      |       |  |
| Frequency Tolerance  |                    |   |     |                      |       |  |
| Initial frequency accuracy <sup>1</sup>  | F <sub>INIT</sub>  | -2  | —   | 2                    | ppm   | Grade S  |
|  |                    | -5  | —   | 5                    | ppm   | Grade D  |
| Temperature stability over full temp range <sup>2</sup>  | F <sub>STAB</sub>  | -5  | —   | 5                    | ppm   | Grade S  |
|  |                    | -20   | —   | 20                   | ppm   | Grade D  |
| Aging  | S <sub>AGING</sub> | -1  | —   | 1                    | ppm/y | Maximum aging slope at 25 °C   |
|  | F <sub>AGING</sub> | -3  | —   | 3                    | ppm   | 10-year aging at 25 °C   |
| <b>Notes:</b>  |                    |   |     |                      |       |  |
| 1. Inclusive of initial frequency tolerance at 25°C, variations over supply voltage, load and humidity after 2 times of reflows. |                    |   |     |                      |       |  |
| 2. Frequency / temperature characteristics with offset removed.  |                    |   |     |                      |       |  |
| IO Characteristics   |                    |   |     |                      |       |  |
| SDA, SCL   | V <sub>IH</sub>    | 0.7×V <sub>DD</sub>   | —   | —                    | V     | Input high voltage   |
|  | V <sub>IL</sub>    | —   | —   | 0.3×V <sub>DD</sub>  | V     | Input low voltage  |
|  | V <sub>OH</sub>    | 0.83×V <sub>DD</sub>  | —   | —                    | V     | Output high voltage  |
|  | V <sub>OL</sub>    | —   | —   | 0.17×V <sub>DD</sub> | V     | Output low voltage   |

Continued on next page

| Parameter   | Symbol      | Min               | Typ  | Max               | Unit     | Note  |
|---|-------------|-------------------|------|-------------------|----------|---|
| <b>Output Characteristics</b>   |             |                   |      |                   |          |   |
| Powerup time  | $T_{OSC}$   | —                 | —    | 4                 | ms       | Time from power reaches $0.9 \times V_{DD}$ to output frequency ( $F_{CLK}$ ) within spec |
| Duty cycle  | DC          | 45                | —    | 55                | %        | All formats   |
| Rise/Fall time<br>(20% to 80% VPP)  | $T_{R/F}$   | —                 | 0.5  | 1.5               | ns       | LVC MOS (Load = 10pF // 10k $\Omega$ )  |
|   |             | —                 | —    | 350               | ps       | Differential (100 $\Omega$ termination)   |
| 0.8V differential   | $V_{OC}$    | 0.15              | 0.20 | 0.25              | V        | Mid-level   |
|   | $V_O$       | 0.70              | 0.80 | 0.90              | $V_{PP}$ | Swing (Diff)  |
| 1.0V differential   | $V_{OC}$    | 0.20              | 0.25 | 0.30              | V        | Mid-level   |
|   | $V_O$       | 0.90              | 1.00 | 1.10              | $V_{PP}$ | Swing (Diff)  |
| 1.2V differential   | $V_{OC}$    | 0.25              | 0.30 | 0.35              | V        | Mid-level   |
|   | $V_O$       | 1.10              | 1.20 | 1.30              | $V_{PP}$ | Swing (Diff)  |
| LVC MOS   | $V_{OH}$    | $0.83 \times V_R$ | —    | —                 | V        | LVC MOS (Load = 10pF // 10k $\Omega$ )  |
|   | $V_{OL}$    | —                 | —    | $0.17 \times V_R$ | V        |   |
| <b>Phase Noise and Jitter</b>   |             |                   |      |                   |          |   |
| RMS jitter<br>BW: 12k - 20MHz   | $R_J$       | —                 | 52   | 70                | fs       | $F_{CLK} \geq 100$ MHz  |
|   |             | —                 | 100  | 200               | fs       | $F_{CLK} \geq 50$ MHz   |
|   |             | —                 | 150  | 300               | fs       | $F_{CLK} < 50$ MHz  |
| Phase noise<br>156.25MHz 0.8V<br>differential output<br>$V_{DD} = 1.8 - 3.3V$ | $PN_{1k}$   | —                 | -137 | —                 | dBc/Hz   | Phase noise at 1kHz offset  |
|   | $PN_{10k}$  | —                 | -148 | —                 | dBc/Hz   | Phase noise at 10kHz offset   |
|   | $PN_{100k}$ | —                 | -155 | —                 | dBc/Hz   | Phase noise at 100kHz offset  |
|   | $PN_{1M}$   | —                 | -162 | —                 | dBc/Hz   | Phase noise at 1MHz offset  |
|   | $PN_{10M}$  | —                 | -163 | —                 | dBc/Hz   | Phase noise at 10MHz offset   |
| <b>PSNR</b>   |             |                   |      |                   |          |   |
| Spurs from power noise<br>50mV ripple<br>$V_{DD} = 1.8V$                      | PSNR        | —                 | -76  | —                 | dBc      | 100 kHz sine wave   |
|   |             | —                 | -75  | —                 | dBc      | 200 kHz sine wave   |
|   |             | —                 | -75  | —                 | dBc      | 500 kHz sine wave   |
|   |             | —                 | -75  | —                 | dBc      | 1 MHz sine wave   |
| Spurs from power noise<br>50mV ripple<br>$V_{DD} = 2.5$ or $3.3V$             | PSNR        | —                 | -83  | —                 | dBc      | 100 kHz sine wave   |
|   |             | —                 | -83  | —                 | dBc      | 200 kHz sine wave   |
|   |             | —                 | -83  | —                 | dBc      | 500 kHz sine wave   |
|   |             | —                 | -82  | —                 | dBc      | 1 MHz sine wave   |

**Table 2.2. Environmental Compliance and Package Information**

| Parameter                        | Value |
|----------------------------------|-------|
| Moisture sensitivity level (MSL) | 3     |

**Notes:**  
For additional product information not listed in the data sheet (e.g. RoHS Certifications, MSDS data, qualification data, REACH Declarations, ECCN codes, etc.), contact [aeonsemi.com/contact\\_us](http://aeonsemi.com/contact_us)

**Table 2.3. Absolute Maximum Ratings<sup>1</sup>**

| Parameter                              | Symbol       | Rating              | Unit |
|--|--------------|---------------------|------|
| Maximum operating temperature          | $T_{AMAX}$   | 125                 | °C   |
| Storage temperature                    | $T_S$        | -55 - 125           | °C   |
| Supply voltage                         | $V_{DD,MAX}$ | -0.5 - 3.8          | V    |
| Input voltage                          | $V_{IN,MAX}$ | -0.5 - $V_{DD}+0.3$ | V    |
| ESD HBM (JESD22-A114)                  | HBM          | 4.0                 | kV   |
| ESD CDM (JESD22-C101)                  | CDM          | 1.0                 | kV   |
| Solder Temperature <sup>2</sup>        | $T_{PEAK}$   | 260                 | °C   |
| Solder time at $T_{PEAK}$ <sup>2</sup> | $T_P$        | 20 - 40             | sec  |

**Notes:**

- Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
- The device is compliant with JEDEC J-STD-020.

### 3. Recommended Output Terminations

#### 3.1. Differential Output

The output drivers support AC-coupled or DC-coupled terminations as shown in figures below.

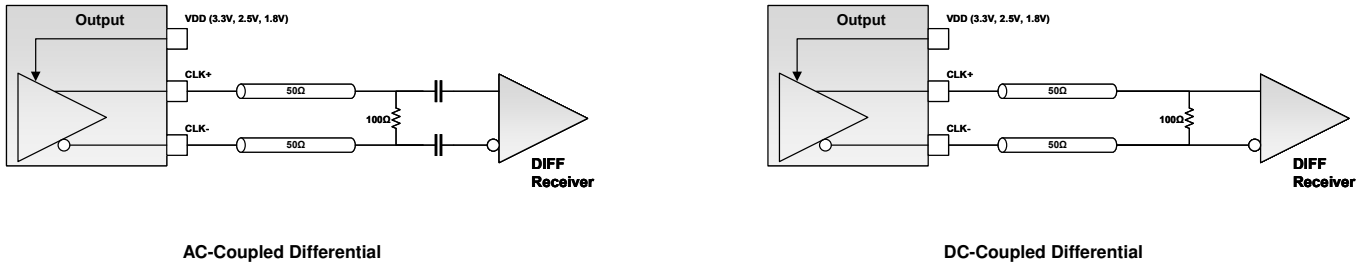


Figure 3.1. Differential Output Terminations

#### 3.2. CMOS Output

Dual CMOS output format options support either complementary or in-phase signals for two identical frequency outputs. This feature enables replacement of multiple XOs with a single AS5223 device.



Figure 3.2. Integrated 1:2 CMOS Buffer Supports In-Phase or Complementary Outputs

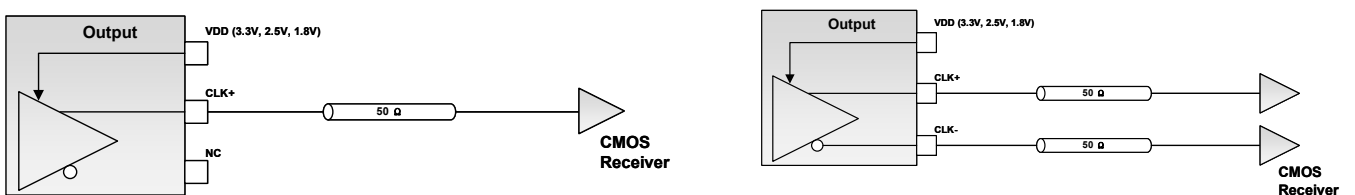


Figure 3.3. LVCMOS Output Terminations

## 4. Configuring via I<sup>2</sup>C Interface

### 4.1. I<sup>2</sup>C Serial Interface

The I<sup>2</sup>C interface on the AS5203 is fully compatible with the “UM10204 I2C-bus specification and user manual, Rev. 6 - 4 April 2014” standard, as described in Table 4.1.

Table 4.1. I<sup>2</sup>C Compatibility

| I <sup>2</sup> C Protocol | Speed   | Compliance | Notes   |
|---------------------------|---------|------------|---|
| Standard                  | 100 kHz | Compliant  | N/A   |
| Fast                      | 400 kHz | Compatible | SDA falling edge can be faster than 20 ns depending on loading.                                       |
| Fast+                     | 1 MHz   | Compatible | SDA falling edge can be faster than 20 ns depending on loading.<br>SDA max pull down current is 6 mA. |

### 4.2. I<sup>2</sup>C Register Write and Read Protocol

AS5203 implements an 8-bit I<sup>2</sup>C address space with 256 addressable byte register locations. Certain device register and bits are reserved, and they must not be changed from their default reset state. In an I<sup>2</sup>C bus system, the AS5203 acts as a slave device connected to the I<sup>2</sup>C serial interface bus. It is accessed via a 7-bit factory programmed (per user specification) slave address. Allowed values of this device address are in the range from 8 to 119. Both write and read register transactions with register address auto increment are enabled as shown in Figure 4.1.

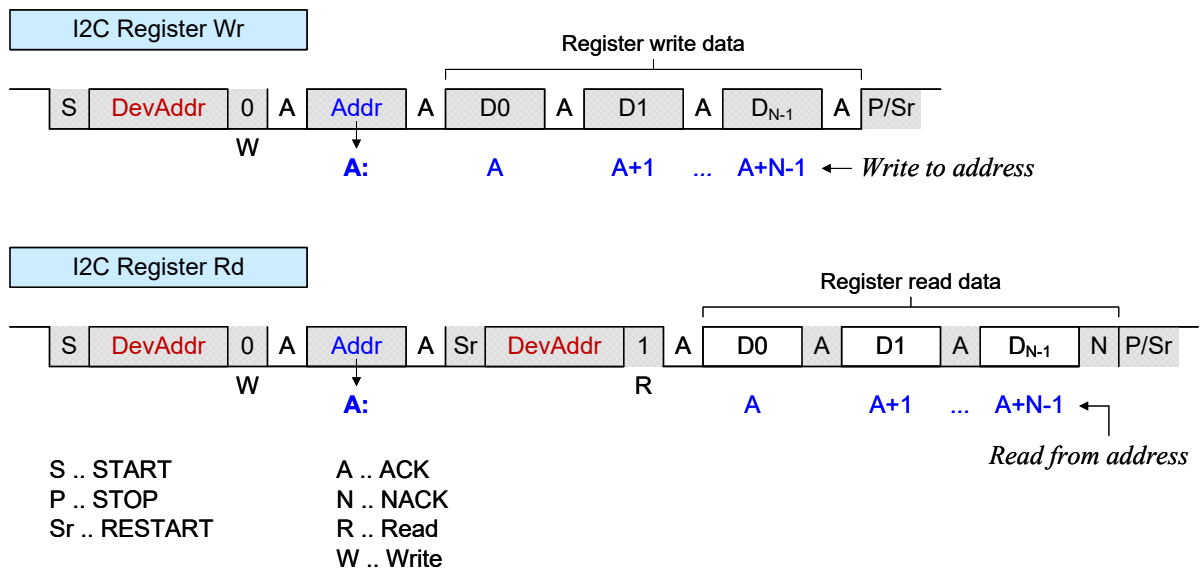


Figure 4.1. I<sup>2</sup>C Write and Read Transactions

Write register transaction is an I<sup>2</sup>C write transaction with an 8-bit register address data byte stream. It is followed by one or more register data bytes. Read register sequence starts after a write transaction to set the read register address. It is followed by the I<sup>2</sup>C read transaction to read one or more data bytes.

The register address autoincrement is enabled upon power up. It is incremented till a maximum address 0xFF of the I<sup>2</sup>C register space is reached.

Data and address bytes appear on the SDA bus with the most significant bit (MSB) first per I<sup>2</sup>C standard. During I<sup>2</sup>C transactions, SCL clock bus is never stalled by the device.

### 4.3. I<sup>2</sup>C Register Reference

The I<sup>2</sup>C interface is a byte-oriented interface. Registers are wider than 8 bits requiring to be split into multiple bytes located on subsequent register addresses. There are two types of multi byte registers:

1. Array of arrays, prefix ab, for example abUSER\_ID[4] are organized in little endian fashion, byte abUSER\_ID[0] is located at the lowest address, and the last byte of the array abUSER\_ID[3] is located at the highest address.
2. An assigned 32-bit long integer, prefix j, and a 32-bit IEEE 754-2008 floating point number, prefix f are organized in big endian fashion, such that the most significant byte (MSB) is located at the lowest address.

Any unassigned byte registers have prefix b. Registers in the I<sup>2</sup>C address space 0x00...0xFF without specifications in the register description table are reserved for factory use. All register bit fields labeled [reserved] are read only and are reserved for factory use. Read value should be ignored. Any register bits not specifically mentioned in "Bits" columns are unused. Writing to these registers is ignored and a read always returns a 0. Numerical values are either hexadecimal with 0x prefix or decimal without any prefix.

Descriptions of register table columns:

**Table 4.2. Register Table Columns**

| Register   | Description   |
|------------|---|
| Addr       | I <sup>2</sup> C register address.  |
| Register   | Register name.  |
| Bytes      | Number of bytes in the register. Wider than single byte registers span several subsequent bytes in an address space.  |
| Endian     | Endian for registers wider than one byte. Not applicable for single byte registers.   |
| B          | Big endian. The most significant byte (MSB) of the register appears at the lowest address.  |
| L          | Little endian. The least significant byte (LSB) of the register appears at the lowest address.  |
| Field      | Field name within the register.   |
| [reserved] | Reserved for factory use and readable only  |
| Bits       | Field bit locations within a register. When the field spans more than one bit, the [M:L] notate. Denoting locations of a most significant bit M and a least significant bit L within the register are used. |
| Type       | Field access type.  |
| R/W        | Read/write field by I <sup>2</sup> C.   |
| R          | Read only field by I <sup>2</sup> C.  |
| W1         | Writing a 1 triggers an associated event, while writing a 0 has no effect. A read always returns 0.   |
| Rst        | Field reset value. The value 'Factory' indicates that the value depends on the individual device factory configuration.   |

#### 4.4. Register Map

The device incorporates a Digital Controlled Oscillator (DCXO) feature to allow seamless and fast setting of the frequency deviation from the center frequency. Table 4.3. shows the DCXO configuration registers.

**Table 4.3. DCXO Configuration Registers**

| Register      | Addr | Field      | Bits   | Type | Rst | Description  |
|---------------|------|------------|--------|------|-----|--|
| dcxo_wdata[4] | 0x8b | wdata      | [31:0] | R/W  | 0   | Frequency offset to write to DCXO in signed 32-bit, big endian format.   |
| dcxo_step[4]  | 0x8f | step       | [31:0] | R/W  | 0   | Frequency step to write to DCXO in signed 32-bit, big endian format.   |
| dcxo_ctrl     | 0x93 | step_dir   | [2]    | R/W  | 0   | Controls the step is applied positively or negatively:<br>0: Down<br>1: Up   |
|               |      | step_apply | [1]    | W1   | 0   | Adds extra offset to the DCXO by the amount of step  |
|               |      | clr        | [0]    | W1   | 0   | Synchronously resets the DCXO DSP.   |
| dcxo_rdata[4] | 0x95 | rdata      | [31:0] | R    | 0   | DCXO data register through which the actual DCXO control data is applied. The data is in signed 32-bit, big endian format. The added frequency per LSB depends on the device's frequency and crystal used. |

5. Package Outline Drawing

Figure 5.1. shows the package outline drawing for the AS5223 devices. Details of dimension for different size options are listed in Table 5.1.

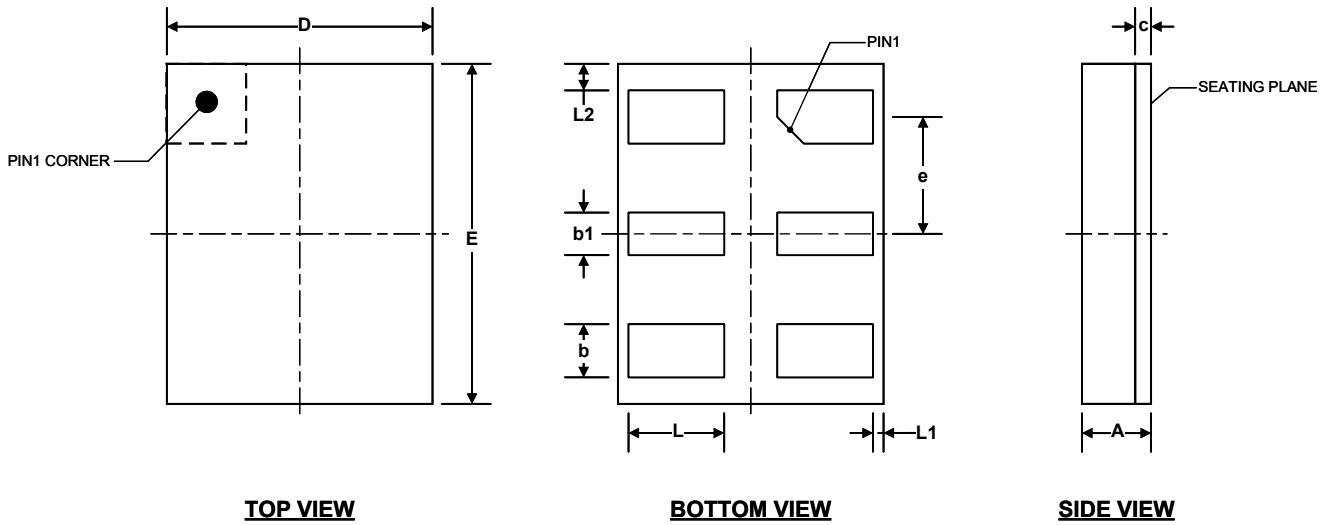


Figure 5.1. Package Outline Drawing

Table 5.1. Dimensions of Package Outline Drawing (mm)

| Symbol | Min   | Nom       | Max   |
|--------|-------|-----------|-------|
| A      | 0.790 | 0.890     | 0.990 |
| b      | 0.225 | 0.300     | 0.375 |
| b1     | 0.225 | 0.300     | 0.375 |
| D      | 1.550 | 1.600     | 1.650 |
| e      | —     | 0.750 BSC | —     |
| E      | 1.950 | 2.000     | 2.050 |
| L      | 0.375 | 0.450     | 0.525 |
| L1     | 0.025 | 0.100     | 0.175 |

## 6. Recommended PCB Land Pattern

Figure 6.1. shows the drawing of recommended PCB land pattern for the AS5223 devices. Details of dimension for different size options are listed in Table 6.1.

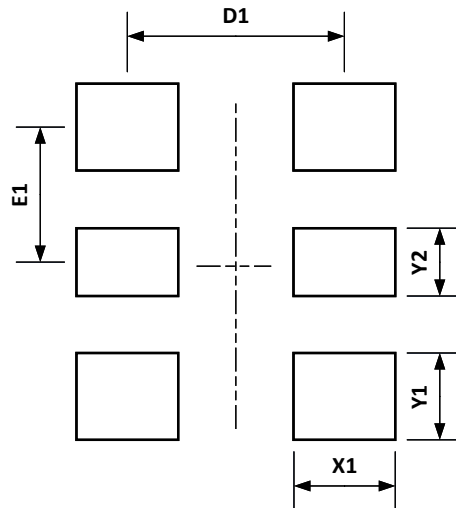


Figure 6.1. Recommended PCB Land Pattern

Table 6.1. Dimensions of Recommended PCB Land Pattern (mm)

| Symbol | 2016 Package |
|--------|--------------|
| D1     | 1.05         |
| E1     | 0.75         |
| X1     | 0.75         |
| Y1     | 0.50         |
| Y2     | 0.50         |

### Notes:

The following notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

### General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

### Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu\text{m}$  minimum, all the way around the pad.

### Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 0.8 1 for the pads.

### Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Top Mark

Figure 7.1. shows the top mark specifications for the AS5223 devices. Description of each line is listed in Table 7.1.

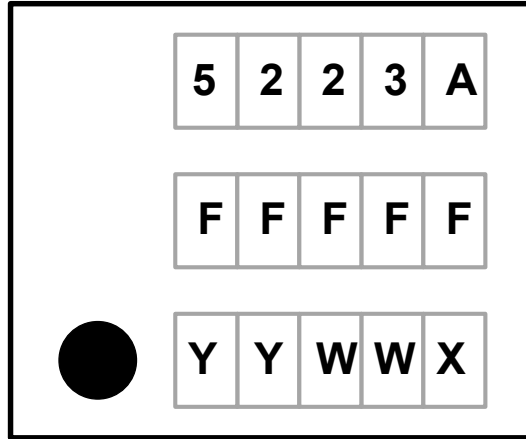


Figure 7.1. Top Mark

Table 7.1. Top Mark Description

| Line | Position | Description   |
|------|----------|---|
| 1    | 1-6      | Device Name   |
| 2    | 1-5      | Unique 5-digit Device Configuration Number  |
| 3    | 1        | Pin 1 orientation mark (dot)  |
|      | 2-3      | Year (last two digits of the year), to be assigned by assembly site (ex: 2025 = 25) |
|      | 4-5      | Calendar Work Week number (1-53), to be assigned by assembly site                   |
|      | 6        | Manufacturer code   |

## 8. Important Notice and Disclaimer

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## 9. Revision History

| Revision | Date     | Description  |
|----------|----------|--|
| 1.03     | Mar 2026 | Updated the Top Mark Rule  |
| 1.02     | Sep 2025 | Corrected several description errors   |
| 1.01     | Aug 2025 | Officially release as mass production version                                      |
| 0.09     | Feb 2025 | Added "2016" package outline diagram   |
| 0.08     | Aug 2024 | Updated several items  |
| 0.07     | Apr 2024 | Remove the package outline drawings temporarily                                    |
| 0.06     | Feb 2024 | Updated the "Ordering guide"   |
| 0.05     | Aug 2023 | Revised the stability for D-grade option   |
| 0.04     | Jul 2023 | Updated the package outline  |
| 0.03     | Jun 2023 | Updated the "Ordering guide" and added phase noise jitter for clock $\geq 100$ MHz |
| 0.02     | Feb 2023 | Updated the "Temperature Stability Grade" D grade                                  |
| 0.01     | Nov 2021 | Preliminary release  |