AN521: Introduction of AS500x Oscillator Frequency Stability

1. Introduction

The AS500x is a silicon-based reference clock generator. Figure 1.1 shows the block diagram: an LC oscillator (LCO) provides the clock input to a low-noise digitally controlled fractional-N frequency generator (FRAC-N); a driver block (DRV) with programmable multi-format outputs conditions the FRAC-N signal for export off-chip. The LCO if left uncompensated, is susceptible to changes in frequency due to environmental variables such as the ambient temperature, supply-voltage and humidity. Additionally, thermal stress incurred during solder-reflow causes large, relatively fast, thermal transients that can result in a frequency shift. This application note quantitatively describes the AS500x's unique but predictable frequency-stability response relative to various environmental stresses and conditions. With the proprietary on-chip compensation scheme, AS500x maintains its output frequency within ±50 ppm of its target value over all such environmental conditions during the operating lifetime.

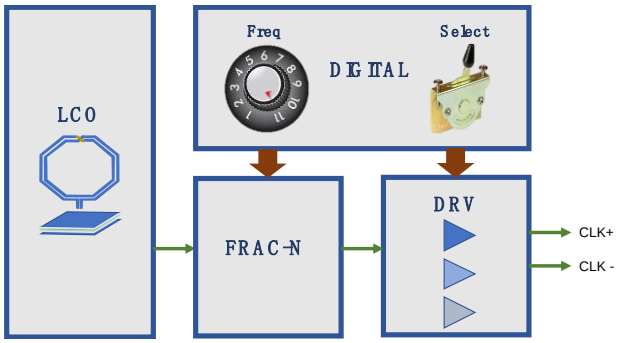

Figure 1.1 Simplified block diagram of AS500x

2. Solder Reflow

The AS500x responds in a systematic manner to a solder reflow event. For best predictability, it is important that the solder-reflow thermal profile be compliant with the JEDEC standard defined in J-STD-020D.1 as summarized in Figure 2.1 and Table 2.1. Note that for Pb-free assembly, Tc = 260 °C for the AS500x and that soldering by hand will not cause the part to malfunction, but lack of control in the solder-reflow heating profile will result in higher variability in the resultant frequency shift.

For the AS500x, a solder-reflow event results in a negative systematic offset in the frequency-error. Immediately after solder reflow the initial frequency error will likely measure below –50 ppm. However, over time, the error will relax upwards and eventually disappear. The fully reversible solder-reflow process for the AS500x is shown in Figure 2.2 as the frequency offset over time. The figure shows a typical post-solder-reflow relaxation curve measured at 20 °C starting just after the solder reflow event. Immediately after solder reflow, the AS500x will typically have a –60 ppm offset relative to its frequency error just prior to solder reflow with a 3.8 ppm standard deviation. After 50 hours, the part will recover half of this error and by 1200 hours, it will recover 90% of the error. After approximately 10000 hours, the error induced by solder reflow will be completely reversed. Subjecting the part to another solder-reflow event restarts this reversible process and another 10000 hours would be needed before the negative offset has again been eliminated. If the temperature at which the solder-reflow relaxation occurs is increased, the time required to fully reverse the frequency offset can be greatly diminished.

For instance, at 100 °C, the offset can be reversed in 24 hours — an improvement of 500 times.

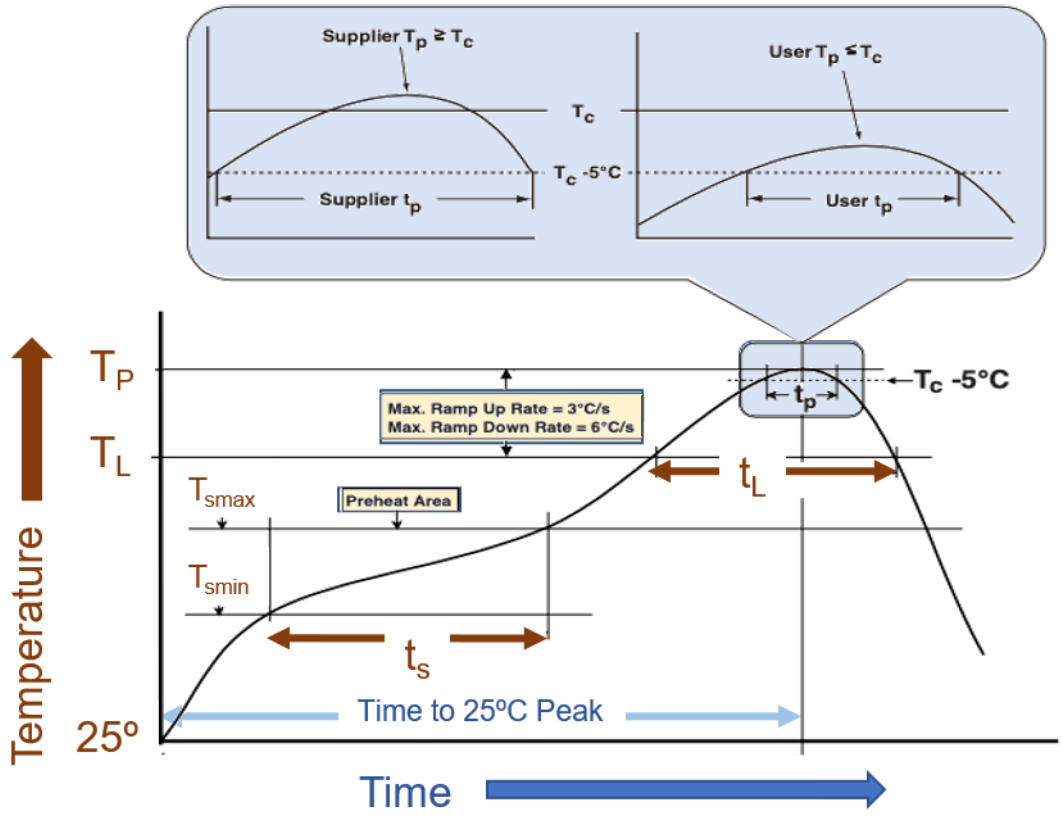

Figure 2.1 JEDEC defined temperature profile during solder reflow for AS500x

Table 2.1 JEDEC solder-reflow parameters reference in Figure 2.1

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Ramp-up rate (TL to Tp)	3 °C/second max.	3 °C/second max.
Liquidous temperature (TL) Time (tL) maintained above TL	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the Classification temp in Table 2A. For suppliers Tp must equal or exceed the Classification temp in Table 2A	For users Tp must not exceed the Classification temp in Table 2B. For suppliers Tp must equal or exceed the Classification temp in Table 2B
Time (tp)* within 5 °C of the specified classification temperature (Tc), see Table 2a & 2B Figure 5-1. J-STD-020D.1	20* seconds	30* seconds
Ramp-down rate (Tp to TL)	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum		

The post-soldered initial frequency error (F_o) at 20 °C for the AS500x is difficult to specify because it is a function of time. If the effect of solder-reflow relaxation is not included, the expected value of F_o is -10 ppm with a standard deviation of 4.2 ppm. At a rate of 10 defects-per-million (DPM), F_o will range between –28 ppm and +8 ppm. Figure 2.2 can be used as a compendium to include the effects of solder-reflow relaxation by adding the predicted offset to F_o based on the elapsed time from the solder-reflow event.

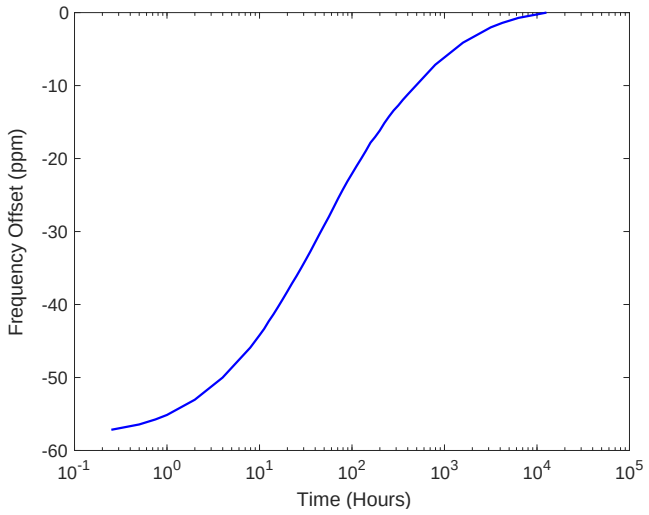

Figure 2.2 Typical solder-reflow relaxation vs. time

3. Temperature Calibration and Sensitivity

The native frequency error vs. temperature for the AS500x, without compensation, could exceed ± 250 ppm (relative to 30°C). Background calibration over the full operating-temperature range from –40°C to 85°C, removes most of this temperature sensitivity. This is accomplished by storing a 4th-order polynomial to the on-chip non-volatile memory (NVM). The polynomial describes the LC output frequency relative to the output of the on-chip temperature sensor. A proprietary and economical technique is used in production on automatic test equipment (ATE) to extract this polynomial for each part individually such that each part has a custom polynomial stored to its on-chip NVM allowing for optimal frequency calibration.

4. Baking After Solder Reflow

Baking the unpowered parts within a few hours of solder reflow at temperatures between 70°C and 105°C (the maximum storage temperature) accelerates the post-solder-reflow frequency relaxation shown in Figure 2.2.

Baking parts in this temperature range can greatly accelerate the post solder-reflow relaxation error and push F_o closer to its target value of -10 ppm as well as reduce the overall standard variation of the frequency error.

5. Thermal Cycling Temperature Between 100°C and –40°C

Repetitively cycling the temperature between 100°C and -40°C (or vice versa) further pushes the frequency error upwards. This effect is termed thermal-cycle-shift and is primarily a systematic error. Figure 5.1 shows the distribution of thermal-cycle shift for 64 devices after 6 complete thermal cycles between 100°C and –40°C. Note that the standard deviation of the distribution is small (1 ppm). Once the part has been thermal cycled a few times, it reaches a steady state where additional thermal cycles no longer cause an upward shift in frequency. Subsequent thermal cycles can then be run to find the expected results for the frequency error over temperature as shown in Figure 5.2 for five hundred devices which includes multiple fabrication process corners.

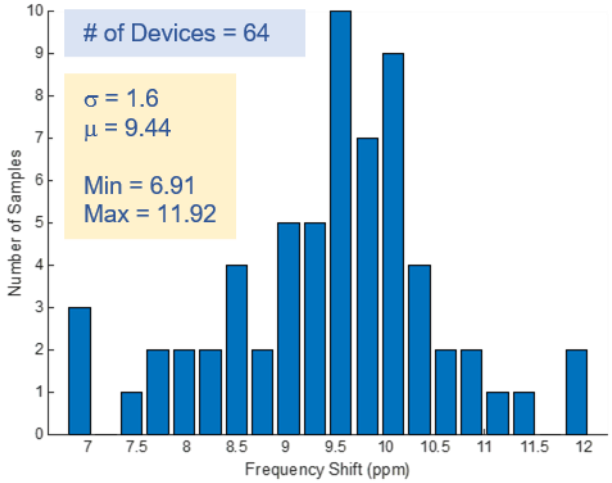

Figure 5.1 Histogram of expected thermal cycle shift

These results plot only the error due to temperature; all errors due to solder-reflow variation, baking or thermal cycling were zeroed out at 30°C. Further, these results are only for parts in 5032 packages, but parts using the 3225 package also have similar results. Notice a small amount of hysteresis occurs as the part is thermal-cycled from 100°C to -40°C and then back to 100°C over a couple hour timeframe. This is evidenced by the small eye that appears in the plot below 30°C. To help see this effect more clearly in Figure 5.2, the average of all the results is shown with the blue line. The jagged nature of the curve is due to the limited number of points that were measured over temperature.

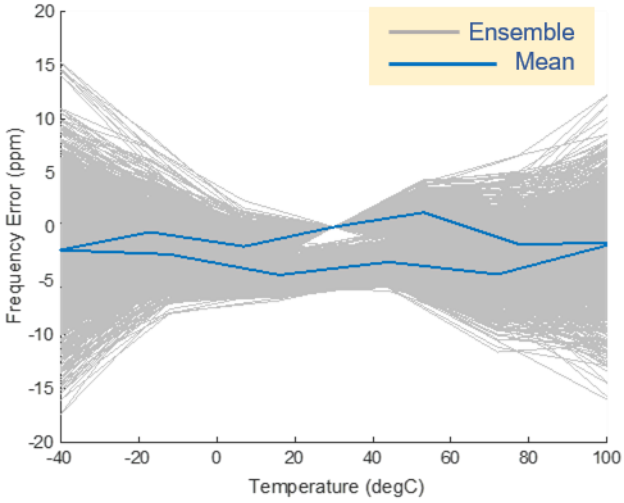

Figure 5.2 Expected frequency error over temperature. Included are various process-corners

6. Power-Supply Sensitivity

The calibration algorithm used to create the 4th-order temperature stability polynomial is optimized at V_{dd} = 2.5 V. If the part is operated at a different supply between 1.7 V and 3.47 V, the frequency error vs. temperature will change slightly. Figure 6.1 shows this in detail. All results are shown normalized to V_{dd} = 2.5; thus, this curve (gray line) shows no error across the entire temperature range for this voltage. The curvature seen in the plots at other supplies is due to small supply-induced

changes to the frequency-vs-temperature polynomial relative to the polynomial that was originally written to the NVM. From 1.7 V to 3 V, this error is mostly within ±2 ppm. Above 3V, errors approaching -8 ppm are observed but only at temperatures below -20°C. From 20°C to 100°C, the errors are better than -4 ppm. As initially freezing the device will also cause a shift upwards in frequency (as part of thermal cycling), there is no concern this power supply sensitivity will impact the overall frequency stability budget.

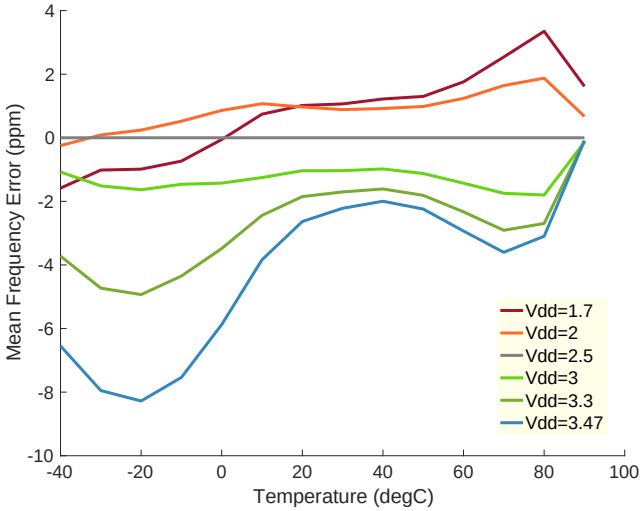

Figure 6.1 Power-supply sensitivity over temperature

7. Humidity Sensitivity

Figure 7.1 shows the measured frequency error over time due to the relative humidity (RH) profile. The RH in the temperature chamber was measured using a humidity sensor. To increase the speed of the humidity response, the experiment was run at T = 90 °C. The initial positive step in humidity seen just after t = 0 hours is due to placing a large container of very hot water in the oven. As a result, the relative humidity in the chamber changes rapidly - more quickly than would be observed during normal operation in the field. The second negative humidity step occurs at approximately t = 34 hours due to all the water evaporating from the initial humidity step. Over the next few hours, the humidity drops close to its original value and the transient due to this RH step is more muted than at first. There is a small increase of frequency seen in Figure 7.1 over time due to aging. This is expected given the high ambient temperature at which the experiment was run. Removing the effects of aging, it is expected that as RH varies from 15% to 85%, the AS500x will experience no more than a ±2 ppm error in its output frequency.

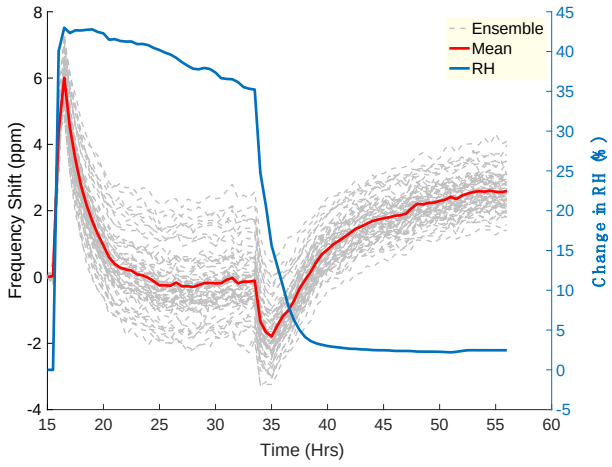

Figure 7.1 Frequency shift due to step changes in the RH profile in the temperature chamber

8. 10-Year Aging

Long-term of aging effects are estimated using the following equation:

$$\text{Aging(ppm)} = 0.78 \log_{10}\left[\frac{\text{T(Years)}}{0.0571}\right] \cdot 10^{0.1072[(T_j - 10)/10]}$$

The aging time (T) is expressed in years and the junction temperature (T_j) in °C. This equation is valid for T greater than 500 hours (0.0571 years) and T_j less than 110°C. Above 110°C, the aging begins to double for every 10°C increase in junction temperature. To avoid this region of operation, the AS500x max storage temperature has been conservatively specified at 105°C.

9. Other Effects

9.1. Long-Term Hysteresis

After solder-reflow and baking at 100°C for several hours, the parts reach a quiescent state where there is no further change observed in the frequency error. If the parts are subsequently returned to room temperature, the frequency error begins to creep upwards with a time constant of several hours. After 50 hours, the parts again reach a steady state with a frequency error that is approximately 12 ppm higher than when they were first measured at room temperature immediately after baking. This is designated as long-term hysteresis and is believed to be related to the relaxation seen after soldering the parts. Just like solder reflow, the process is reversible. After the parts reach steady state at room temperature, baking at 100°C will reverse the upward shift and the process will repeat itself once the parts are returned to room temperature. The details of the upward frequency shift over time are shown in Figure 9.1.

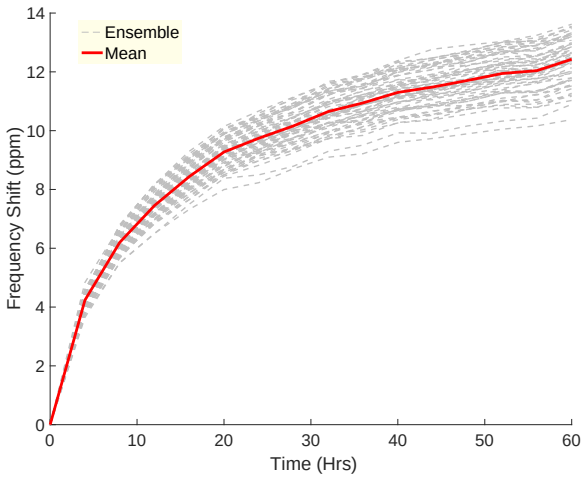

Figure 9.1 Room temperature frequency shift over time after baking device at 100 ºC. This is designated as long-term hysteresis.

9.2. Frequency Pulling

Due to the proprietary design of the on-chip LC oscillator, the frequency sensitivity of the AS500x to metal being brought into proximity with the die (or even being placed on top of the package) is minimal. Further, the output frequency is largely invariant to changes in impedance on the various chip I/O. This includes effects from toggling the I/O from one state to the other or changing the trace length on the GPIO pins. The frequency sensitivity to either of these effects has been demonstrated to be less than 1 ppm.

9.3. Shock and Vibration

Due to the pure electric nature of the resonator that doesn't contain any mechanical elements, the AS500x can sustain extremely high shock and vibration without risk of device failure. Tests with shock and vibration up to 40G across a range of frequencies in the X-Y-Z directions showed less than 1 ppm of frequency error under all conditions.

10. Summary

The AS500x is designed to remain within ±50 ppm of its target frequency over a wide variety of environmental and operating conditions. To help the user quantify their expected frequency-error range given their custom set of operating conditions, a spreadsheet is available to automate the calculations. The spreadsheet asks, as input, for the following: max/min ambient temperature, supply voltage, max/min relative humidity, expected aging- time and temperature. To quantify the frequency-error offset due to solder reflow relaxation, the spreadsheet also asks for the number of elapsed hours since the solder reflow event. The spreadsheet returns an estimate of the maximum and minimum frequency error (in ppm) and the expected frequency-error offset due to solder-reflow relaxation.

11. Revision history

Rev	Date	Description
1.0	May 2021	- Initial release