AN522: AS5001 in High-Speed Serial Link Applications

1. Introduction

This application note describes the function of the reference clock in typical high-speed serial link applications such as 56G / 100G PAM-4 DSP, CDR and re-timer. Analysis of the reference clock's stability and jitter requirement is shown and followed with conclusions.

2. Serial link overview

Serial link transceivers are often referred as SerDes (Serializer and De-serializer) when a high-speed serial data stream such as 56Gbps is converted into multiple parallel lower speed data stream such as 25 Gbps. When the input and output data rates are the same, the device is often called re-timer. In both cases, the transceiver cleans up the amplitude and timing noise in the incoming signal and sends out higher quality data stream in its respective data format such as NRZ or PAM-4.

The receiver performs the function of recovering clock and data embedded in the incoming signal, hence is also called CDR. CDR architecture has evolved in recent years as data rate increases. One of the popular architectures found in the leading products in the market is the ADC-based digital architecture due to its versatility in dealing with a wide range of channels in 56Gbps and 112Gbps PMA-4 systems. This ADC-based PAM-4 CDR is sometimes referred as PAM-4 DSP. Regardless ADC based CDR or analog based CDR, the clock recovery architecture is very similar as described below.

3. Clock Recovery Loops in CDR

Unlike the single loop CDRs in early days, recent CDRs use dual loop architecture to decouple CDR loop bandwidth and transmit jitter transfer bandwidth. As a result, receiver jitter tolerance performance and transmit jitter filtering can be optimized independently at the same time. Figure 3.1 shows a simplified diagram of a 56 Gbps PAM-4 CDR using such architecture. There are three timing loops in the transceiver. First, a reference PLL taking an external 156.25MHz reference clock and generates an internal high frequency T-clock (14GHz or 28GHz); Second, a CDR DLL loop tracks closely the phase of the incoming data by controlling the phase delay added to the internal T-clock; Lastly, a frequency tracking loop forces the internal T-clock to be synchronous to the incoming data by controlling the fractional feedback of the reference PLL.

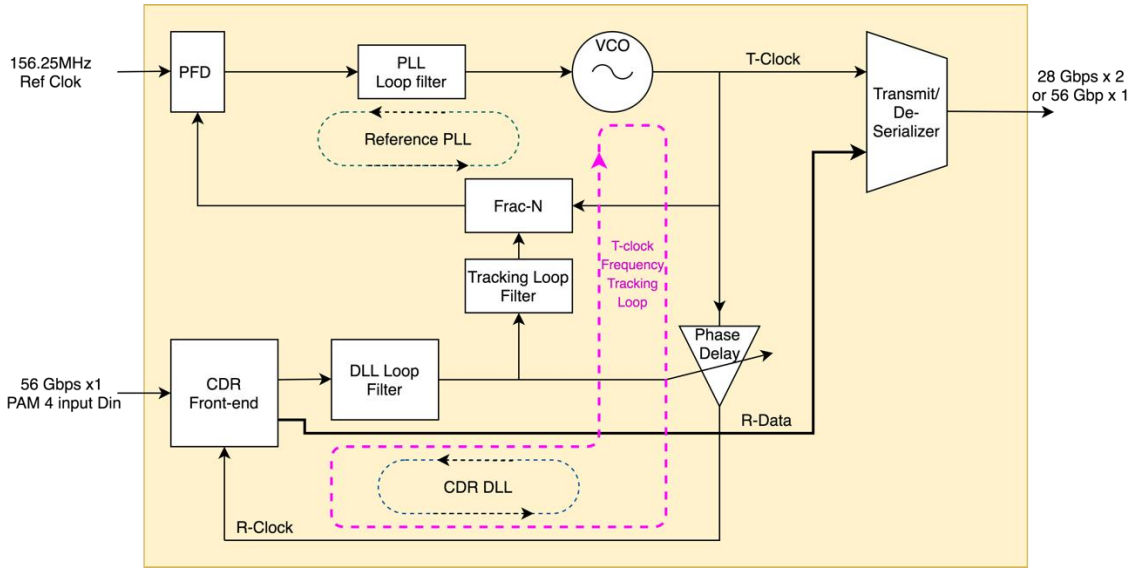

Figure 3.1 Simplified block diagram of a 56 Gbps PAM-4 CDR / DSP

4. Jitter Transfer Function of the Clock Recovery Loops

To understand the requirements of reference clock, it is important to examine the jitter transfer characteristics of the various timing paths given the interaction between reference PLL, CDR DLL and the frequency tracking loop.

4.1. Data input Din to CDR Recovered Clock (R-Clock) Jitter Transfer

In order to recover the input data reliably in the presence of channel impairments induced large jitter, the receive clock R-Clock needs to track the phase of the incoming data closely to sample the data signal at an optimal timing instance. As such, the CDR DLL loop is usually designed to have high bandwidth so that high frequency jitter can be tracked out. Figure 4.1 illustrate the typical jitter transfer function of CDR PLL and its corresponding jitter tolerance.

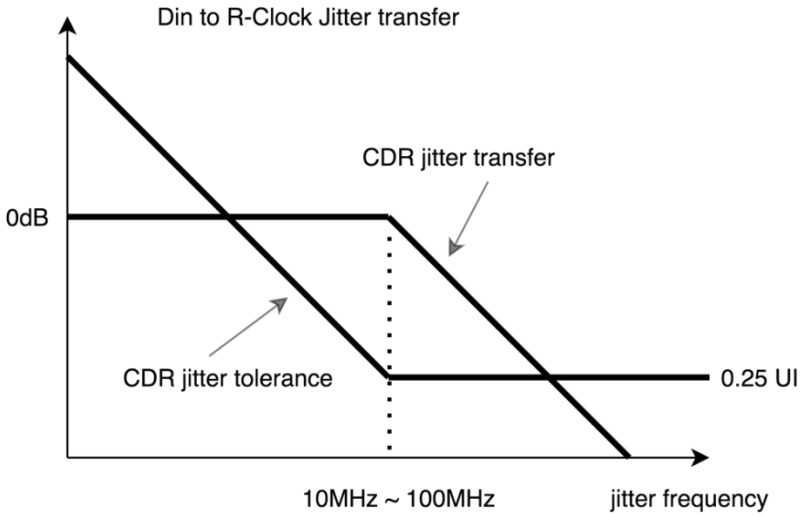

Figure 4.1 Data input to R-Clock jitter transfer function and CDR jitter tolerance

4.2. Reference Clock to CDR Recovered Clock (R-Clock) Jitter Transfer

The reference PLL generates a high frequency T-Clock based on the input reference with initial frequency very close to the target frequency of the data rate. The CDR DLL then takes this clock and applies phase delay adjustment to align with the phase of the incoming data. Note that phase-interpolator based DLL can achieve data lock even when there is a frequency error in T-Clock. The pull in range of these types of DLL is usually on the order of 1,000ppm. Most lower data rate NRZ CDR can operate without a reference clock.

The jitter from T-clock enters into R-clock with a high-pass transfer function, and jitter from reference clock enters into R-clock with a bandpass function as illustrated in Figure 4.2. Due to DLL's relatively high bandwidth of 10MHz, the jitter from reference clock to R-Clock is largely suppressed, as a result, the CDR is only sensitive to the reference clock jitter in a very narrow band.

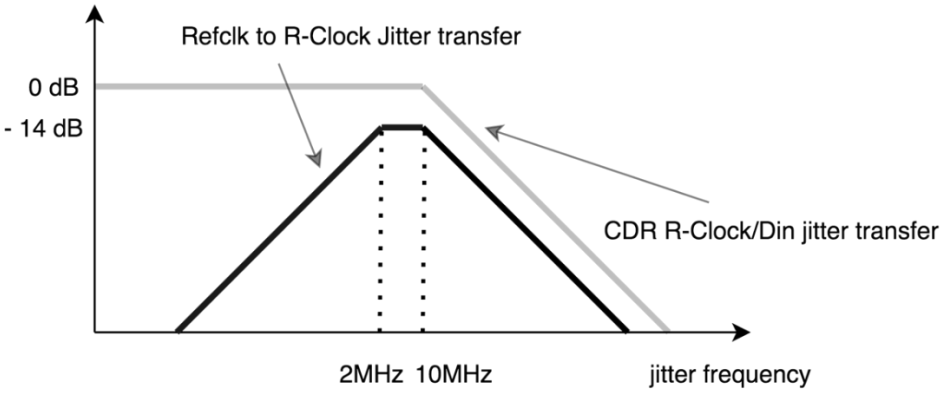

Figure 4.2 Reference clock to CDR R-Clock jitter transfer

4.3. Reference Clock to Transmit clock (T-Clock) Jitter Transfer

Without the T-clock frequency tracking loop, the jitter transfer from reference clock to T-clock would be a lowpass filter just like in a regular PLL as illustrated with the dashed line in Figure 4.3. With the frequency tracking loop, T-clock tracks the frequency of the incoming data Din with a bandwidth around 100kHz to a few hundred KHz. Consequently, the resulting transfer function of reference clock to T-clock is a band-pass filter as illustrated in Figure 4.3.

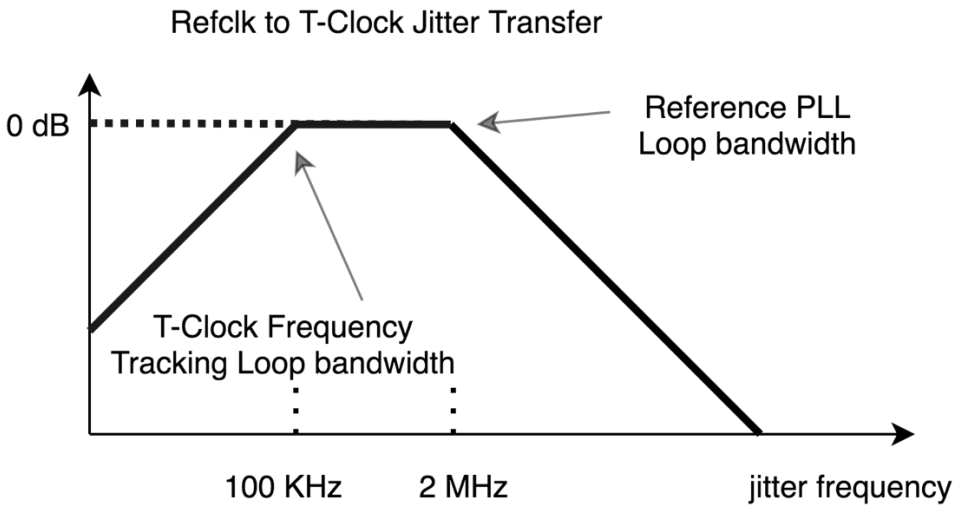

Figure 4.3 Reference clock to Transmit clock jitter transfer

5. Jitter and Stability of Reference Clock in Serial Link Applications

The industry has been using 12kHz to 20MHz as the common frequency band when specifying clock jitter. This jitter band came from SONET (Synchronous Optical Network) system which is not as applicable these days in data center and Ethernet applications. A more accurate evaluation of the jitter can be done by applying the jitter transfer function to the reference clock phase noise.

Taking AS5001 156.25MHz output phase noise as an example shown in Figure 5.1, and assuming a conservative low tracking bandwidth of 100kHz (most design has tracking loop greater than 200kHz), the resulting integrated jitter contribution from AS5001 reference clock is less than 50 fs rms. This 50 fs compared with 56Gbps PAM4 symbol unit interval (UI) of 35ps is less than 0.15% and should be well within spec.

Frequency stability is another important spec for clocks. For serial link application, the reference clock provides an initial starting frequency for CDR to acquire lock. After CDR lock is achieved, the frequency of the data and corresponding timing paths are synchronous to the incoming data, hence the frequency stability requirement of the reference clock is only needed to allow CDR to acquire lock. As mentioned earlier, CDR's frequency pull in range is on the order of 1,000 ppm, hence the frequency stability of the reference clock is very forgiving. Usually 100 ppm can provide more than adequate design margin. AS5001 can meet the requirement easily.

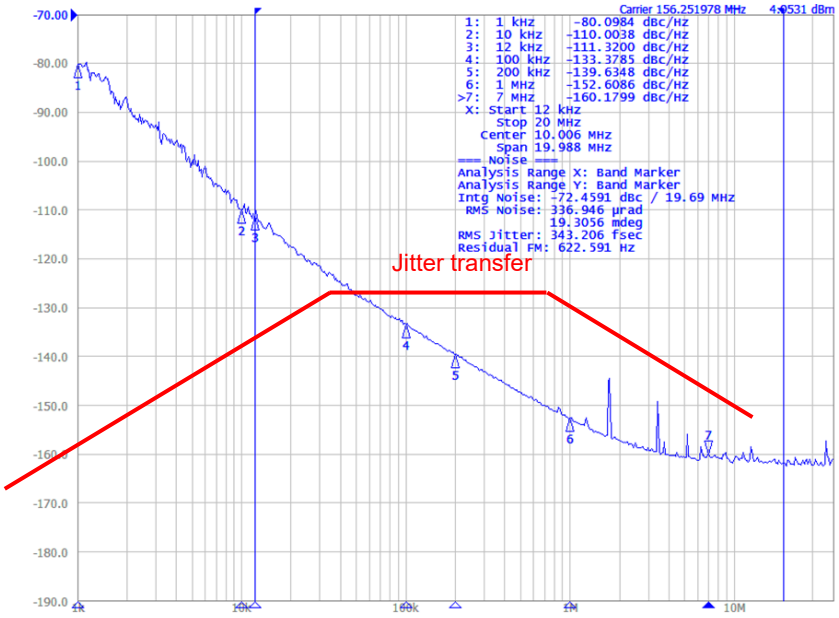

Figure 5.1 AS5001 Phase Noise and T-Clock Jitter Transfer

6. Conclusion

By analyzing the internal architecture of the 56 Gbps PAM-4 and 100 Gbps PAM-4 CDR, we conclude that the reference clock jitter in this application should be specified in the band of 100 kHz to 10 MHz instead of 12kHz to 20MHz. AS5001 is a perfect solution in high-speed serial link applications due to its superior jitter performance in the band of interest, and its robustness and reliability based on its monolithic CMOS integration technology.

7. Revision history

Rev	Date	Description of Changes
1.0	April 4, 2021	Initial revision