AN523: AS500x Power Supply Noise Rejection

1. Introduction

The AS500x is a family of industry-leading high-performance all-silicon oscillator. Benefitting from its integrated Low Drop-Out (LDO) linear voltage regulator, AS500x series maintains great jitter performance in the presence of moderate power supply noise. Figure 1.1 shows the simplified block diagram of AS500x. An LDO is integrated on chip to suppress the effect of external power supply noise. This application note presents the test data showing AS500x's superior power supply noise rejection performance.

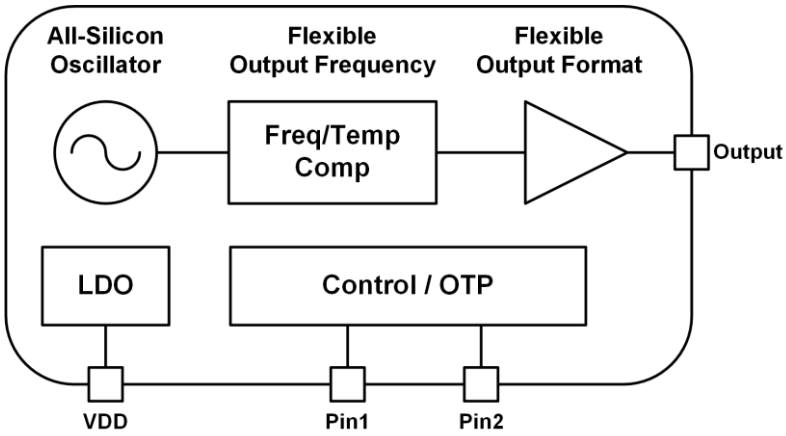

Figure 1.1 Simplified block diagram of AS500X

2. Overview of Power Supply Noise Test setup

To characterize the effect of power supply noise on AS500x, a test was conducted to evaluate how the phase noise of AS500x output clock reacts to the power supply noise.

Figure 2.1 shows the simplified schematic of test setup:

- Power supply to test the DUT under wide operating range of Vdd from 1.7V to 3.3V
- RF signal generator superimposes noise signal at various frequencies with 50mV$_{pp}$ on power supply using a Bias Tee.
- SMA connection from Bias Tee to AS500X DUT board is terminated with 50ohm resistor to ground at board.
- Only 0.1uF bypass capacitor is placed at AS500X VDD pin on DUT board.
- Balun is used to interface between AS500X DUT board and phase noise analyzer.

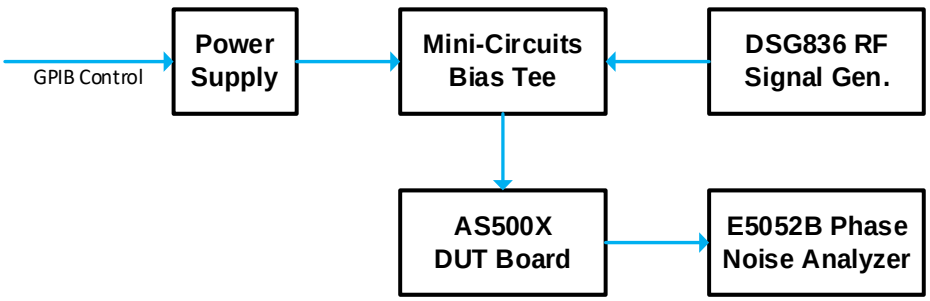

Figure 2.1 Simplified schematic of test setup

3. Test Method and Example Result

In general, the power supply noise affects the output clock performance by crosstalk in frequency domain, which can be captured as spurs in phase noise plot. In most applications, switching power supply is preferred to be used than LDO because it has higher power efficiency, but it adds power supply noise typically from the switching noise. For example, the 100 kHz switching frequency may result in spurs at 100 kHz offset and 100 kHz's integer multiples in frequency domain.

To quantify the effects of power supply noise on AS500x output clock, this test methodology uses DSG836 RF signal generator to simulate the single-tone noise and uses E5052B phase noise analyzer to capture the spurs and calculate the contribution of these spurs to 12k ~ 20 MHz integrated phase noise RMS jitter.

Figure 3.1 shows the example phase noise plot of AS500x output clock when 50mV$_{pp}$ 100 kHz sine wave signal is added on 3.3V power supply at AS500x VDD.

Note: The spurs to the right of 1MHz offset accounts for the "Non-VDD Spur Jitter" in following analysis.

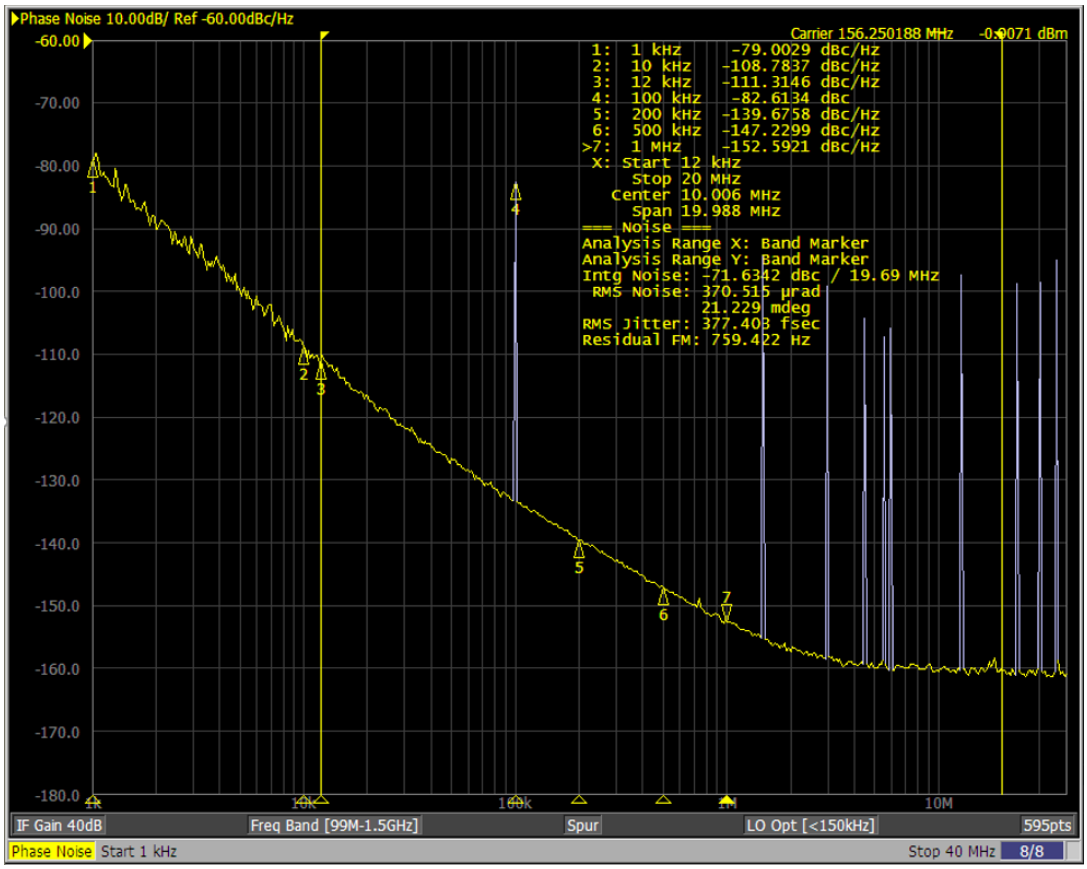

Figure 3.1 Example Phase Noise Plot

4. Result Summary

Table 4.1 shows the result summary of power supply noise test. Measurements are taken under various conditions of noise frequency and power supply level.

Table 4.1 Power Supply Noise Test Results

Power Supply Noise Test Results												
50mVpp Noise frequency	**100 kHz**			**200 kHz**			**500 kHz**			**1MHz**		
AS500x power supply	**1.7V**	**2.5V**	**3.3V**	**1.7V**	**2.5V**	**3.3V**	**1.7V**	**2.5V**	**3.3V**	**1.7V**	**2.5V**	**3.3V**
VDD Spur (dBc)	-76.1	-82.8	-82.8	-75	-82.8	-82.8	-74.7	-82.6	-82.7	-74.5	-82.1	-82.1
VDD Spur Jitter (fs rms)	226	104	104	254.9	104.5	103.9	264.7	106.8	106	271.5	113.6	113.4
Non-VDD Spur Jitter (fs rms)	47.3	46.8	46.6	46.9	46.9	49.7	52.6	49.2	46.7	46.6	52.6	53.4
Jitter w/o Spurs (fs rms)	331.7	341.4	353.4	330.8	333.6	346.6	330.6	333.9	348	336.8	333.1	340
Jitter w/ Spurs (fs rms)	404.4	360	371.4	420.2	352.7	365.2	426.8	353.1	366.8	435.1	355.9	373.3

Notes:

- VDD Spur (dBc): Measured output spur level in dBc due to the 50 mVpp sinusoidal noise (100 kHz, 200 kHz, 500 kHz or 1MHz) added on the VDD supply.
- VDD Spur Jitter (fs rms): Equivalent jitter converted from the measured output spur due to the added noise on VDD supply
- Non-VDD Spur Jitter (fs rms): There were several additional spurs present at higher frequencies. This represents their contribution to the total jitter.
- Jitter w/o Spurs (fs rms): This is the total integrated jitter from 12KHz to 20MHz after removing all spur energy.
- Jitter w/ Spurs (rs rms): This is the total integrated jitter from 12KHz to 20MHz including all spurs.

5. Conclusion

The power supply noise test results demonstrate that AS500x is very robust against power supply noise. 50mVpp supply noise adds less than 100 fs of jitter. AS500x is a perfect solution in systems where high quality clock is required in presence of supply noise.

6. Revision history

Rev	Date	Description
1.0	July 2021	- Initial release