AS5002 Arcadium™ Pin Selectable Frequency Oscillator, 10 kHz to 350 MHz

The AS5002 Arcadium™ all-silicon oscillator utilizes proprietary frequency synthesis and sensor technologies to provide a quartz-free, MEMS-free, low jitter clock at any output frequency. The device is factory-programmed to have 3 selectable frequencies ranging from 10 kHz to 350 MHz with <0.026 ppb resolution and maintains low jitter across its operating range. The AS5002 uses on-chip temperature and strain sensors, and an advanced LC tank architecture to achieve excellent reliabilities even in high impact shock scenarios.

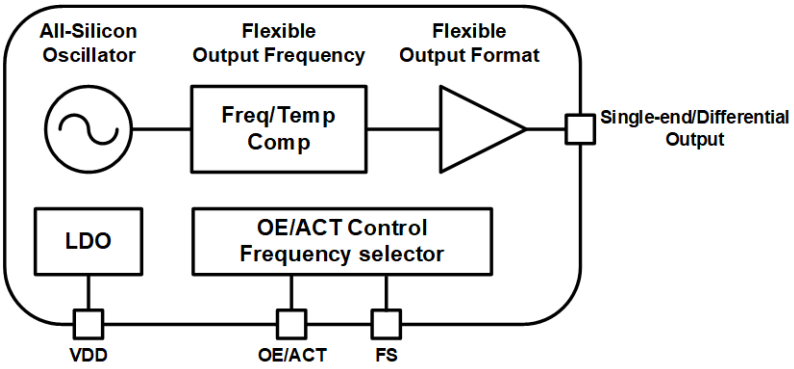
AS5002's on-chip power supply filtering provides industry-leading power supply noise rejection, simplifying the task of generating low jitter clocks in noisy systems that use switched- mode power supplies. Offered in a variety of industry-standard packages, the AS5002 has a dramatically simplified supply chain that enables Aeonsemi to ship samples shortly after receipt of order. The AS5002 is factory-configurable for a wide variety of user specifications, including frequency, output format, and OE pin location. Specific configurations are factory programmed at time of shipment, eliminating the long lead times associated with custom oscillators. This process also guarantees 100% electrical testing of every device before shipment.

KEY FEATURES

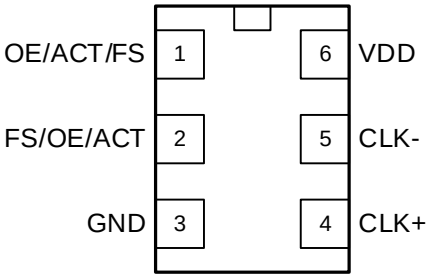
- Quartz-free and MEMS-free without mechanical moving parts
- Flexible output frequency and format; user selectable
- Differential: 10 kHz to 350 MHz
- CMOS: 10 kHz to 212.5 MHz
- LVPECL, LVDS, CML, HCSL, CMOS, or Dual CMOS output options
- Low jitter: 350 fs Typ RMS (12 kHz – 20 MHz)
- Compliant to PCIe Gen 1/2/3/4/5/6 jitter requirements
- Temperature stability:
  - ± 20 ppm (-20 to 85 °C)
  - ± 35 ppm (-40 to 85 °C)
  - ± 35 ppm (-40 to 105 °C)
- Integrated LDO for on-chip power supply noise filtering
- Support 1.8V, 2.5V, 3.3V V_{DD} power supply operation
- Industrial standard 3225 and 5032 package footprints

APPLICATIONS

- 1G/10G/40G/100G/200G Ethernet
- Servers, switches, storage, NICs, search acceleration
- Test and measurement
- Clock and data recovery
- FPGA/ASIC clocking



Pin Assignments



Top view

5032 and 3225 package

Pin #	Descriptions
1, 2	*Selectable via ordering option* OE = Output Enable. Active High ACT = Device Active. Active High FS = Freq selector. Hi-z, High or Low
3	GND = Ground
4	CLK+ = Clock output
5	CLK- = Complementary clock output
6	VDD = Power supply

1. Ordering Guide

The AS5002 Oscillator supports a variety of options including frequency, output format, and FS / OE / ACT pin location, as shown in the chart below. Specific device configurations are programmed into the part at time of shipment, and samples are available in 2 weeks.

XO Series	Description
5002	Pin Selectable

	Device Type
A	General
B	Factory defined setting

	Package
A	5032
B	3225

	Temperature Grade
I	-40 to 85 °C
E	-40 to 105 °C

5002	A	A	-	-	-	-	-	A	B	I	R

	PIN#1	PIN#2
A	OE	FS
B	FS	OE
C	ACT	FS
D	FS	ACT
E	Customized	Customized

Configuration Code[1]	Description
xxxxx	Five digit numeric code

Three pin-selectable settings can be specified within the supported frequency range and signal formats.
A unique five digit numeric code will be assigned for the specific combination of settings.

Device Revision

Code	Packing type	Qty
T	7-inch reel	250
R	13-inch reel	2500
<blank>	Bulk	Sample

Notes:

1. The five-digit numeric code is an identification of the configurations. Check the datasheet appendix for the details

2. Control Pins

2.1. Overview

The AS5002 is a pin selectable oscillator that generates reference clocks with any output frequencies (10 kHz – 350 MHz), and any output formats (LVPECL, LVDS, CML, HCSL, CMOS, or Dual CMOS). Control pins, Pin 1 and Pin 2, of the AS5002 are designed as multi-functional input pins that support various functions, such as output enable (OE), device active (ACT) and frequency select (FS).

2.2. Configuration Selection

The on chip Non-Volatile Memory (NVM) stores three pre-programmed output frequencies and formats. It selects an output frequency and format using the frequency select pin (FS). Configurations can be preset at aeonsemi.com/as5002/customize.

Table 2.1. shows an example of a configuration.

Table 2.1. A Configuration Example with 3 Pre-Programmed Presets

Preset	FS (Pin 1 or Pin 2)	Output Frequency	Output Format
1	Low	156.25 MHz	LVDS
2	Hi-Z	74.25 MHz	Dual CMOS
3	High	50 MHz	LVCMOS

Notes:

AS5002 supports an option of up to 9 different configurations, including FS, ACT, OE and SSC (Spread Spectrum Clock) features on the control pins. Contact aeonsemi.com/contact-us/ for the advanced configurations.

3. Electrical Specifications

Table 3.1. Electrical Specifications

V_{DD} = 1.8 V, 2.5 or 3.3 V ± 5%, T_A = -40 to 105 °C

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Temperature Range	T_A		-40	—	105	°C
Frequency Range	F_{CLK}	LVPECL, LVDS, CML, HCSL	0.01	—	350	MHz
		CMOS	0.01	—	212.5	MHz
Supply Voltage	V_{DD}		1.71	—	3.47	V
Supply Current (F_{CLK} = 50 MHz)	I_{DD}	Tristate Hi-Z (OE = 0)	—	40	50	mA
		Ready State (ACT = 0)	—	1	2	mA
		LVPECL (Standard)	—	70	80	mA
		LVPECL (Self-Biased)	—	60	70	mA
		LVDS	—	45	55	mA
		HCSL	—	60	70	mA
		CML	—	60	70	mA
		Single CMOS (C_L = 15 pF)	—	40	55	mA
		Dual CMOS (C_L = 15 pF)	—	50	60	mA
Temperature Stability[1]	F_{STAB}	-20 to +85°C	-20	—	+20	ppm
		-40 to +85°C	-35	—	+35	ppm
		-40 to +105°C	-35	—	+35	ppm
Frequency offset[2]	F_{OFFSET}	At 25°C	-15	—	+15	ppm
Rise/Fall Time (20% to 80% V_{PP})	T_R/T_F	LVPECL / LVDS / CML	—	—	350	ps
		CMOS (C_L = 15 pF)	—	0.5	1.5	ns
		HCSL, F_{CLK} >50 MHz	—	—	550	ps
Duty Cycle	DC	All formats	45	—	55	%
Output Enable (OE)[3]	V_{IH}	—	0.7×V_{DD}	—	—	V
	V_{IL}	—	—	—	0.3×V_{DD}	V
	T_D	Output Disable Time, F_{CLK} >10 MHz	—	—	3	µs
	T_E	Output Enable Time, F_{CLK} >10 MHz	—	—	20	µs
Output Enable (ACT)[3]	V_{IH}	—	0.7×V_{DD}	—	—	V
	V_{IL}	—	—	—	0.3×V_{DD}	V
	T_D	Output Disable Time, F_{CLK} >10 MHz	—	—	3	µs
	T_S	Device standby time, F_{CLK} >10 MHz	—	—	40	µs
	T_E	Output Enable Time, F_{CLK} >10 MHz	—	—	400	µs
Frequency Select (FS)[4]	V_{IH}		0.7×V_{DD}	—	—	V
	V_{IL}		—	—	0.3×V_{DD}	V
Powerup Time	T_{OSC}	Time from 0.9 × V_{DD} until output frequency (F_{CLK}) within spec	—	—	4	ms

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
LVPECL Output Option[5] (Standard)	V_{OC}	Mid-level	V_{DD}-1.55	V_{DD}-1.4	V_{DD}-1.25	V
	V_O	Swing (diff)	1.35	1.6	1.85	V_{PP}
LVPECL Output Option[5] (Self-Biased)	V_O	Swing (diff)	1.35	1.6	1.85	V_{PP}
LVDS Output Option[6]	V_{OC}	Mid-level (2.5 V, 3.3 V V_{DD})	1.125	1.20	1.275	V
		Mid-level (1.8 V V_{DD})	0.78	0.85	0.92	V
	V_O	Swing (diff)	0.64	0.8	0.96	V_{PP}
HCSL Output Option[7] (R_{term} = 50 Ω)	V_{OC}	Mid-level	0.35	0.4	0.45	V
	V_O	Swing (diff)	1.28	1.6	1.92	V_{PP}
HCSL Output Option[7] (R_{term} = 42.5 Ω)	V_{OC}	Mid-level	0.35	0.4	0.45	V
	V_O	Swing (diff)	1.29	1.62	1.94	V_{PP}
CML Output Option	V_{OC}	Mid-level	V_{DD}-0.35	V_{DD}-0.4	V_{DD}-0.45	V
	V_O	Swing (diff)	1.28	1.6	1.92	V_{PP}
CMOS Output Option	V_{OH}	I_{OH} = 8/6/4 mA for 3.3/2.5/1.8V V_{DD}	0.83×V_{DD}	—	—	V
	V_{OL}	I_{OL} = 8/6/4 mA for 3.3/2.5/1.8V V_{DD}	—	—	0.17×V_{DD}	V

Notes:

1. Frequency / temperature characteristics with offset removed.
2. Inclusive of initial frequency tolerance at 25°C, 10-year aging at 25°C, and variations over supply voltage, load and humidity after soldering-reflow shift settles.
3. OE/ACT includes a 50 kΩ pull-up to V_{DD} for OE/ACT active high. NC (No Connect) pin includes a 50 kΩ pull-down to GND.
4. FS includes a 50 kΩ pull-up to V_{DD} and a 50 kΩ pull-down to GND.
5. R_{term} = 50 Ω to V_{DD} - 2.0 V (see Figure 5.1.)
6. R_{term} = 100 Ω (differential) (see Figure 5.2.)
7. R_{term} = 50/42.5 Ω to GND (see Figure 5.4.)

Table 3.2. Clock Output Phase Jitter and PSRR

V_{DD} = 1.8 V, 2.5 or 3.3 V ± 5%, T_A = -40 to 105 °C

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Phase Jitter (RMS, 12 kHz - 20 MHz)[1,2]	ϕ_J	Differential Formats	—	350	750	fs
F_{CLK} ≥ 10 MHz		CMOS, Dual CMOS	—	350	—	fs
Phase Jitter (RMS, 50 kHz - 20 MHz)	ϕ_J	Differential Formats	—	150	250	fs
F_{CLK} ≥ 100 MHz		CMOS, Dual CMOS	—	100	—	fs
Spurs Induced by External Power Supply Noise	PSRR	100 kHz sine wave	—	-76	—	dBc
50 mV_{PP} Ripple		200 kHz sine wave	—	-75	—	
LVDS 156.25 MHz Output		500 kHz sine wave	—	-75	—	
V_{DD} = 1.8 V		1 MHz sine wave	—	-75	—	
Spurs Induced by External Power Supply Noise	PSRR	100 kHz sine wave	—	-83	—	dBc
50 mV_{PP} Ripple		200 kHz sine wave	—	-83	—	
LVDS 156.25 MHz Output		500 kHz sine wave	—	-83	—	
V_{DD} = 2.5 or 3.3 V		1 MHz sine wave	—	-82	—	

Notes:

1. Applies to output frequency: 50, 100, 156.25, 212.5, 350 MHz.
2. Guaranteed by characterization. Jitter inclusive of any spurs.

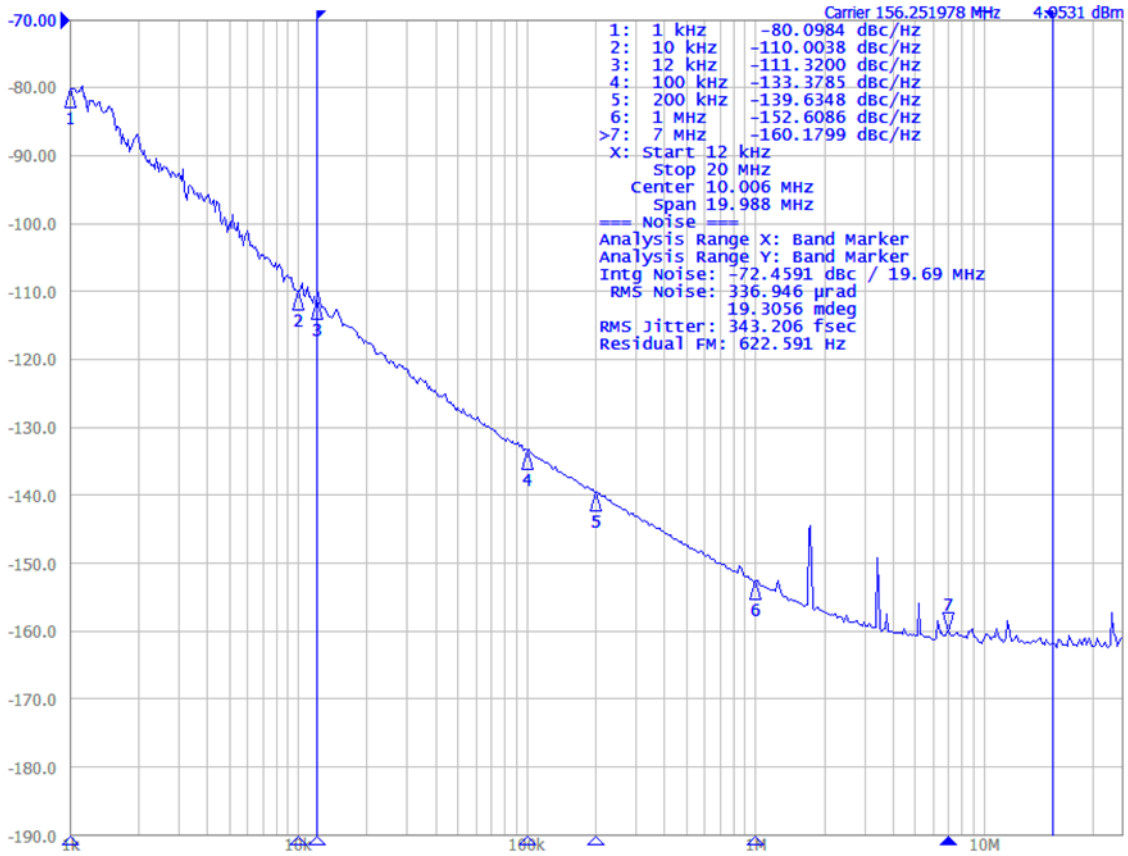


Figure 3.1. Phase Noise at 156.25 MHz

Table 3.3. PCI-Express Clock Outputs (100 MHz HCSL)

VDD = 1.8 V, 2.5 or 3.3 V ± 5%, TA = -40 to 105 °C

Parameter	Test Condition	Specification	Max	Units
PCIe Gen 1.1	Includes PLL BW 1.5 - 22 MHz Peaking = 3dB, T_D=10 ns	N/A	0.311	ps
PCIe Gen 2.1	Includes PLL BW 5MHz & 8 - 16 MHz Peaking = 0.01 - 1 dB & 3 dB, T_D=12ns Low Band, F < 1.5 MHz	3.1	0.022	ps
	Includes PLL BW 5MHz & 8 - 16 MHz Peaking = 0.01 - 1 dB & 3 dB, T_D=12ns High Band, 1.5 MHz < F < Nyquist	3.0	0.259	ps
PCIe Gen 3.0 Common Clock	Includes PLL BW 2 - 4 MHz & 5 MHz Peaking = 0.01 - 2dB & 1dB, T_D=12 ns CDR = 10 MHz	1	0.085	ps
PCIe Gen 4.0 Common Clock	Includes PLL BW 2 - 4 MHz & 5 MHz Peaking = 0.01 - 2dB & 1dB, T_D=12 ns CDR = 10 MHz	0.5	0.085	ps
PCIe Gen 5.0 Common Clock	Includes PLL BW 500 kHz - 1.8 MHz Peaking = 0.01 – 2dB, T_D=12 ns CDR = 20 MHz	0.15	0.033	ps
PCIe Gen 6.0 Common Clock	Includes PLL BW 500 kHz – 1 MHz Peaking = 0.01 – 2dB, T_D=12 ns CDR = 10 MHz	0.1	0.021	ps

Class	Data Rate	Architecture	Specs	Max HF RMS	Max LF RMS	Max Pk-Pk	Compliance Summary
GEN1	2.5 Gb/s	Common Clock	1.1 2.1 3.1	310.77 fs	41.59 fs	N/A	N/A
GEN2	5 Gb/s	Common Clock	1.1 2.1 3.1	259.42 fs	21.89 fs	N/A	All PASS
GEN3	8 Gb/s	Common Clock	3.1 4.0	84.54 fs	4.68 fs	N/A	All PASS
GEN4	16 Gb/s	Common Clock	4.0	84.54 fs	4.68 fs	N/A	All PASS
GEN5	32 Gb/s	Common Clock	5.0	32.92 fs	2.09 fs	N/A	All PASS
GEN6	64 Gb/s	Common Clock	6.0	21.00 fs	0.88 fs	N/A	All PASS

Figure 3.2. PCI-Express clock Compliance Summary

Table 3.4. Environmental Compliance and Package Information

Parameter	Test Condition
Moisture Sensitivity Level	2

Notes:

For additional product information not listed in the data sheet (e.g. RoHS Certifications, MSDS data, qualification data, REACH Declarations, ECCN codes, etc.), contact aeonsemi.com/contact_us

Table 3.5. Thermal Conditions

Package	Parameter	Symbol	Test Condition	Value	Unit
5032 6-pin DFN	Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air	105	°C/W
	Thermal Resistance Junction to Board	Θ_{JB}	Still Air	81	°C/W
	Max Junction Temperature	T_J	Still Air	125	°C
3225 6-pin DFN	Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air	108	°C/W
	Thermal Resistance Junction to Board	Θ_{JB}	Still Air	84	°C/W
	Max Junction Temperature	T_J	Still Air	125	°C

Table 3.6. Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Unit
Maximum Operating Temp	T_{AMAX}	105	°C
Storage Temperature	T_S	-55 to 105	°C
Supply Voltage	V_{DD}	-0.5 to 3.8	V
Input Voltage	V_{IN}	-0.5 to V_{DD} + 0.3	V
ESD HBM (JESD22-A114)	HBM	4.0	kV
ESD CDM (JESD22-C101)	CDM	1.0	kV
Solder Temperature[2]	T_{PEAK}	260	°C
Solder Time at T_{PEAK}[2]	T_P	20 - 40	sec

Notes:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. The device is compliant with JEDEC J-STD-020.

4. CMOS Buffer and Output Terminations

Dual CMOS output format ordering options support either complementary or in-phase signals for two identical frequency outputs. This feature enables replacement of multiple XOs with a single AS5002 device.

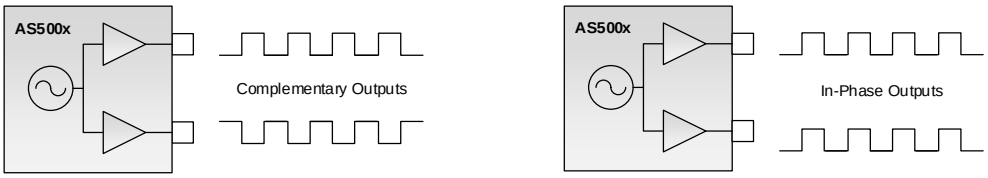


Figure 4.1. Integrated 1:2 CMOS Buffer Supports In-Phase or Complementary Outputs

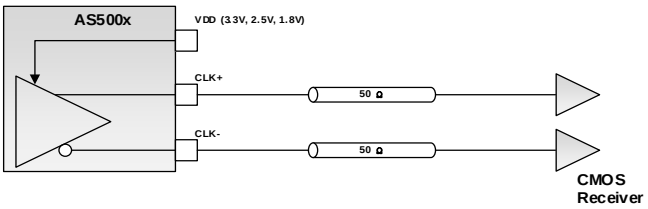


Figure 4.2. Dual CMOS termination

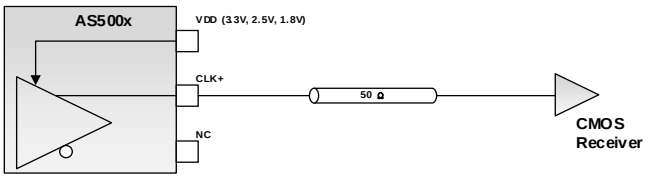
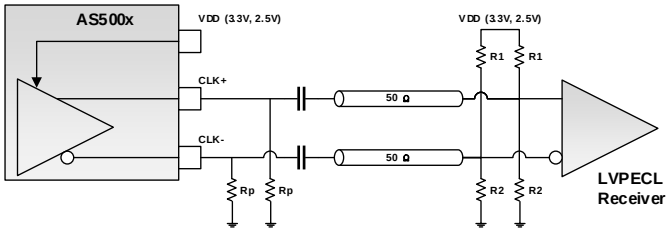


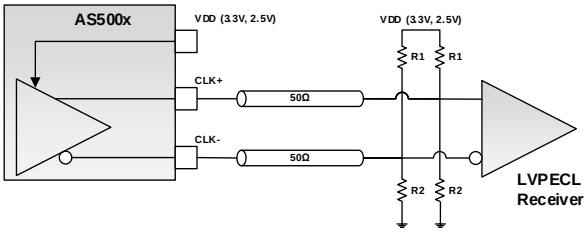
Figure 4.3. Single CMOS termination

5. Recommended Output Terminations

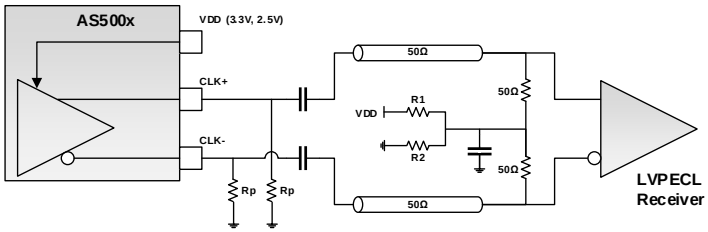
The output drivers support AC-coupled or DC-coupled terminations as shown in figures below.



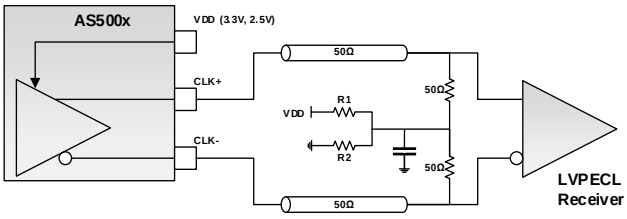
AC-Coupled LVPECL - Thevenin Termination



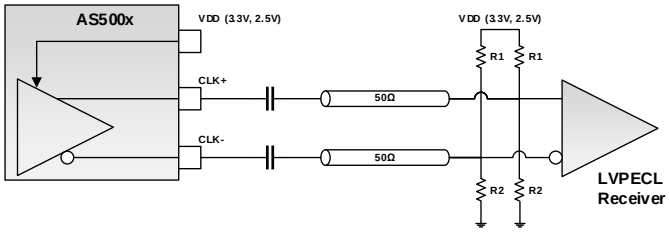
DC-Coupled LVPECL - Thevenin Termination



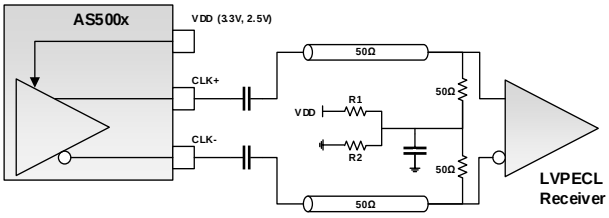
AC-Coupled LVPECL - 50 Ω w/VTT Bias



DC-Coupled LVPECL - 50 Ω w/VTT Bias



AC-Coupled Self-Biased LVEPCL - Thevenin Termination



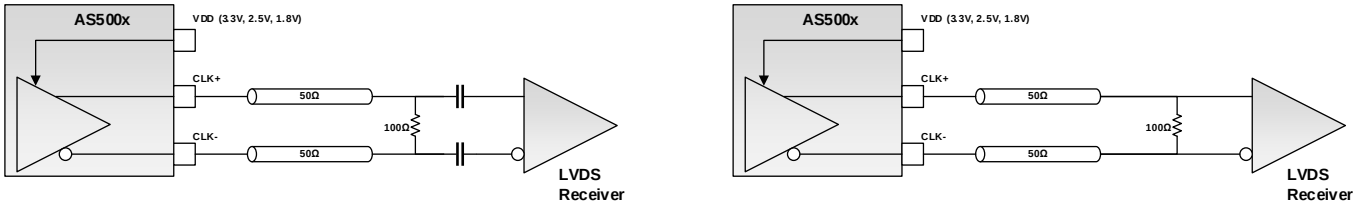
AC-Coupled Self-Biased LVEPCL - 50 Ω w/VTT Bias

Figure 5.1. LVPECL Output Terminations

Table 5.1. LVPECL Termination Resistor Values

AC Coupled LVPECL Termination Resistor Values			
V_{DD}	R_p	R_1	R_2
3.3 V	158 Ω	127 Ω	82.5 Ω
2.5 V	92 Ω	250 Ω	62.5 Ω

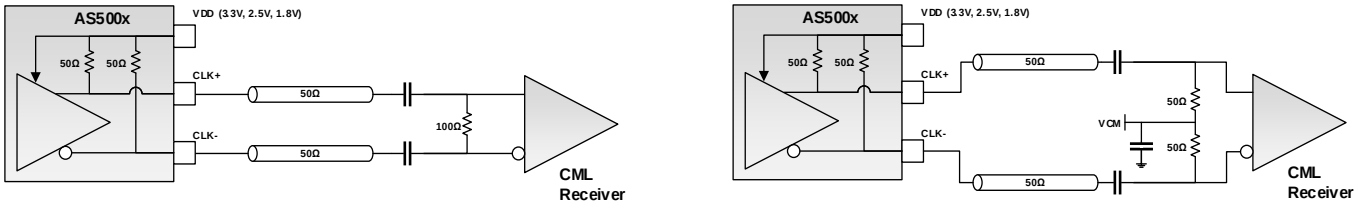
DC Coupled LVPECL Termination Resistor Values		
V_{DD}	R_1	R_2
3.3 V	127 Ω	82.5 Ω
2.5 V	250 Ω	62.5 Ω



AC-Coupled LVDS

DC-Coupled LVDS

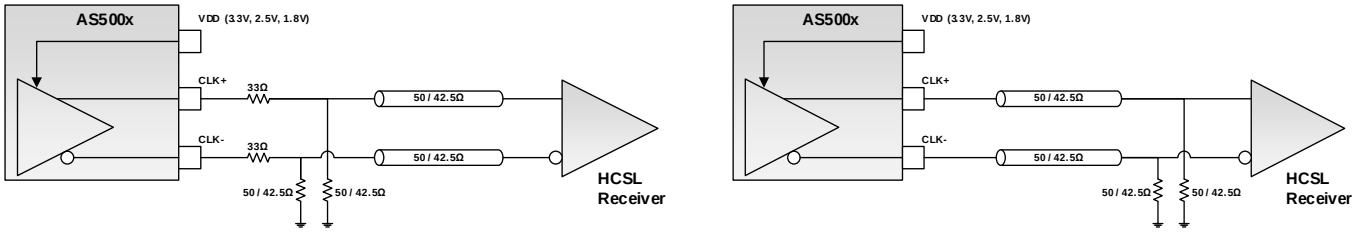
Figure 5.2. LVDS Output Termination



AC-Coupled CML without VCM

AC-Coupled CML with VCM

Figure 5.3. CML Output Termination



Source Terminated HCSL

Destination Terminated HCSL

Figure 5.4. HCSL Output Termination

6. Package Outline

1.1. Package Outline (5032)

The figure below illustrates the package details for the AS5002 devices in 5032 package. The table below lists the values for the dimensions shown in the illustration.

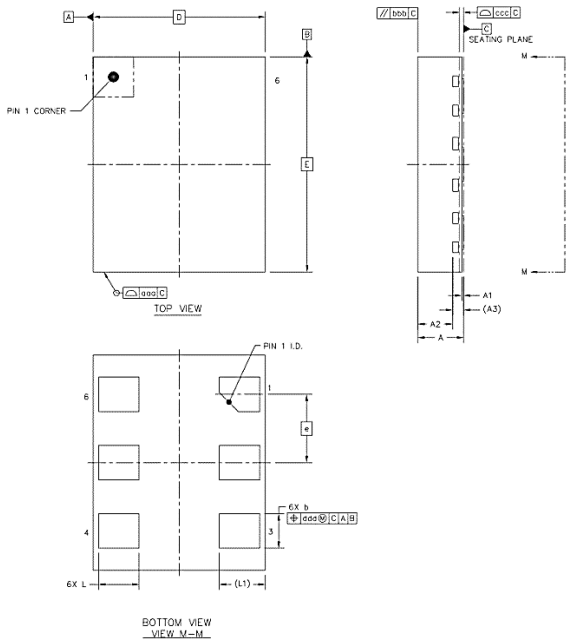


Figure 6.1. AS5002 5032 Package Outline Diagram

Table 6.2. Package Diagram Dimensions (mm)

Symbol	Min	Nom	Max
A	0.8	0.85	0.9
A1	0	0.035	0.05
A2	---	0.65	---
A3	0.203 REF		
b	0.59	0.64	0.69
D	3.1	3.2	3.3
E	3.9	4	4.1
e	1.27 BSC		
L	0.7	0.75	0.8
L1	0.85 REF		
aaa	0.1		
bbb	0.1		
ccc	0.08		
ddd	0.1		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

1.2. Package Outline (3225)

The figure below illustrates the package details for the AS5002 devices in 3225 package. The table below lists the values for the dimensions shown in the illustration.

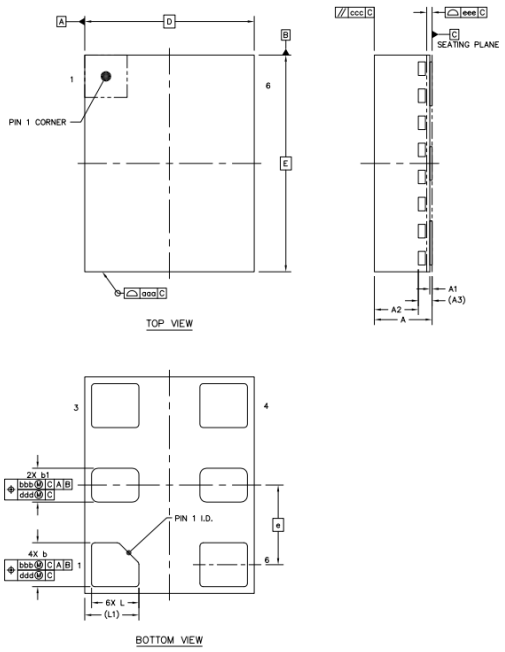


Figure 1.1. AS5002 3225 Package Outline Diagram

Table 1.1. Package Diagram Dimensions (mm)

Symbol	Min	Nom	Max
A	0.8	0.85	0.9
A1	0	0.035	0.05
A2	---	0.65	---
A3		0.203 REF	
b	0.6	0.65	0.7
b1	0.45	0.5	0.55
D	2.4	2.5	2.6
E	3.1	3.2	3.3
e		1.175 BSC	
L	0.65	0.7	0.75
L1		0.8 REF	
aaa		0.1	
bbb		0.07	
ccc		0.1	
ddd		0.05	
eee		0.08	

Notes:

1. All dimensions in millimeters (mm).
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

7. PCB Land Pattern (5032 and 3225 package)

The figure below illustrates the PCB land pattern for the AS5002. The table below lists the values for the dimensions shown in the illustration.

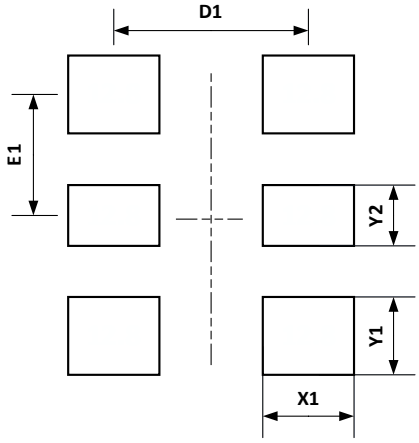


Figure 7.1. AS5002 (5032 and 3225 package) PCB Land Pattern

Table 7.2. PCB Land Pattern Dimensions (mm)

Dimension	Description	5032 Package Value (mm)	3225 Package Value (mm)
X1	Width - leads on long sides	0.80	0.75
Y1	Height - leads on long sides	0.69	0.7
Y2	Height - leads on long sides	0.69	0.55
D1	Pitch in X directions of XLY1 leads	2.30	1.65
E1	Lead pitch XLY1 leads	1.27	1.175

Notes:

The following notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 0.8:1 for the pads.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Top Marking (5032 and 3225 Package)

The figure below illustrates the mark specification for the AS5002. The table below lists the line information.

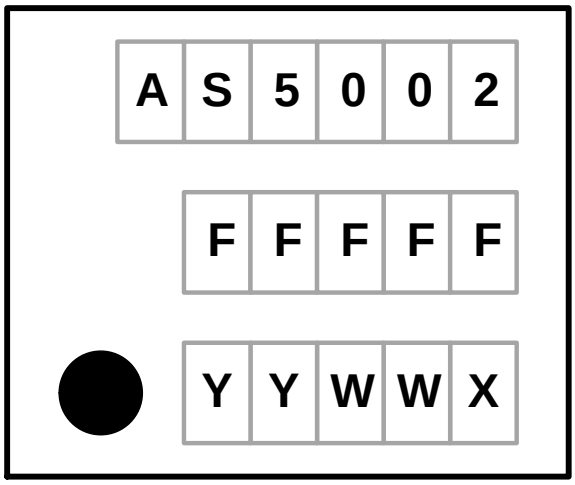


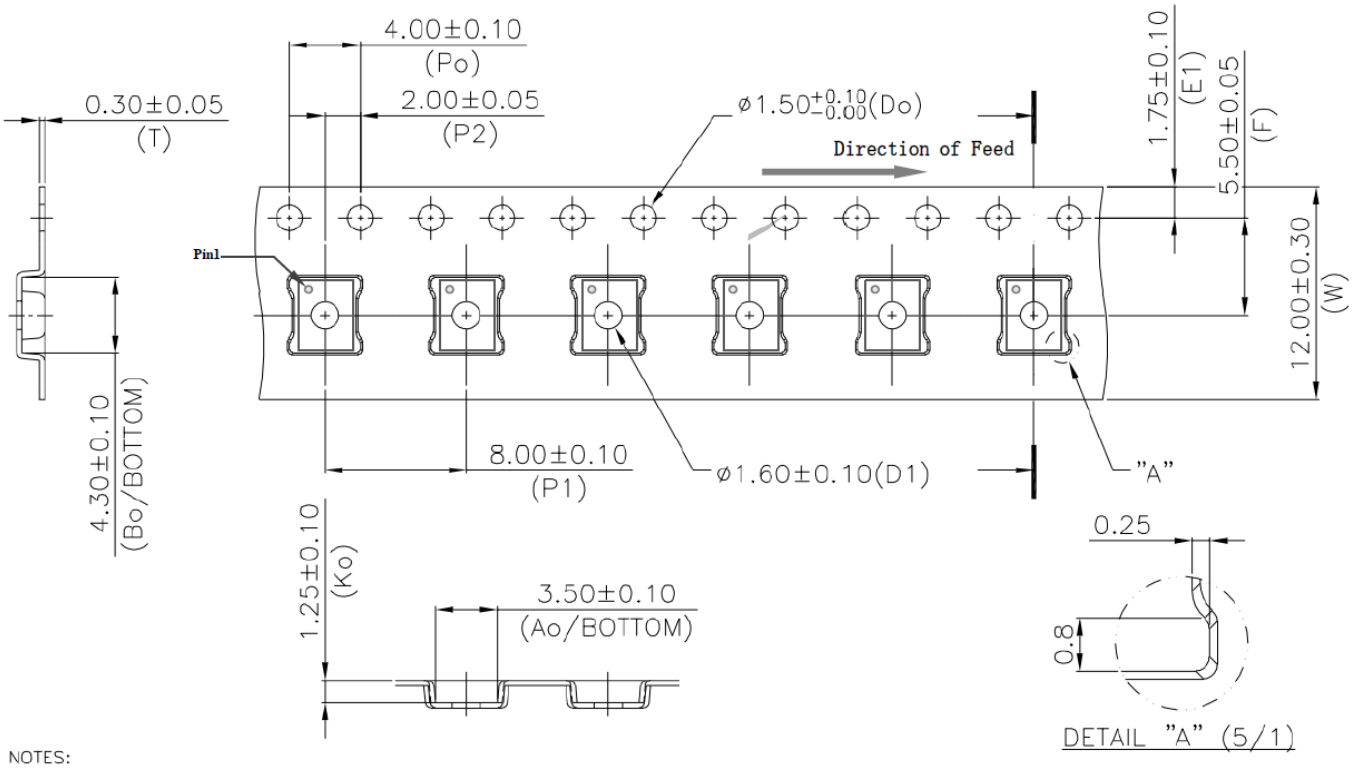
Figure 8.1. AS5002 Top Mark

Table 8.2. AS5002 Top Mark Description

Line	Position	Description
1	1-6	Device Name
2	1-5	Unique 5-digit Device Configuration Number
3	Position 1	Pin 1 orientation mark (dot)
	Position 2-3	Year (last two digits of the year), to be assigned by assembly site (ex: 2017 = 17)
	Position 4-5	Calendar Work Week number (1-53), to be assigned by assembly site
	Position 6	Assembly site code

9. Packing specification

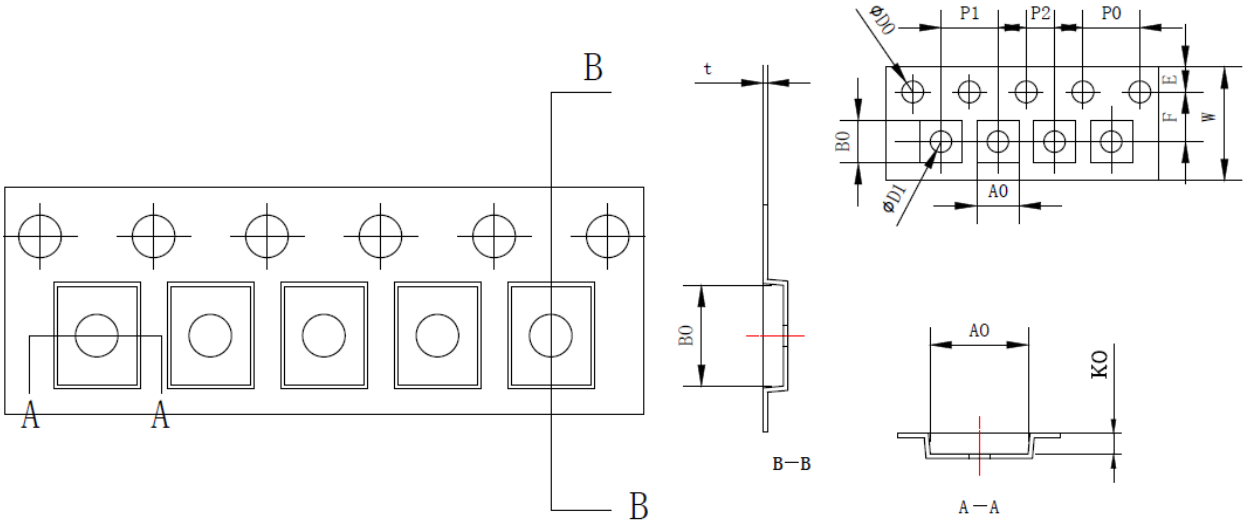
9.1. Tape & Reel (5032)



NOTES:
1. DIM IN mm.
2. 10 SPROCKET HOLE PITCHES CUMULATIVE TOLERANCE ±0.20 mm.
3. CAMBER NOT TO EXCEED 1 mm IN 250 mm.
4. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
5. (S.R. ohms/sq.) MEANS SURFACE RESISTIVITY OF THE CARRIER TAPE. (EIA-541 STANDARD)
6. DIMENSIONS IN ACCORDANCE WITH EIA-481 SPECIFICATIONS.

Figure 9.1. AS5002 5032 Package Packing Specification

9.2. Tape & Reel (3225)



W	E	F	D0	D1	P0	P2	10P0	P1	A0	A1	B0	B1	K0	K1	t
8.00 ±0.30	1.75 ±0.10	3.50 ±0.05	1.50 +0.10	1.00 +0.10	4.00 ±0.10	2.00 ±0.10	40.00 ±0.20	4.00 ±0.10	2.80 ±0.10		3.60 ±0.10		1.10 ±0.10		0.30 ±0.05

Figure 9.2. AS5002 3225 Package Packing Specification

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11. Revision History

Rev	Date	Description
1.12	Aug 2024	Add packing specification
1.11	Mar 2024	Updated the frequency offset
1.10	Jul 2022	Updated the top mark specification Updated the Package Outline and PCB Land Pattern Dimensions for 3225 package Add min/max value of symbol “D” & “E” for package outline
1.01	Dec 2021	Adjusted the PCB land pattern dimensions
1.00	Sep 2021	With certain specification update
0.95	Jun 2021	Corrected the Ordering Guide Insert -40~105oC temperature range option Insert section “PCIe clock compliance” Insert section “IMPORTANT NOTICE AND DISCLAIMER”
0.94	Mar 2021	Updated the Ordering Guide
0.93	Feb 2021	Corrected the Top Mark Corrected the storage temperature
0.92	Feb 2021	Corrected the PCB Land Pattern description Corrected the Top Mark description Updated the Ordering Guide
0.91	Oct 2020	Removed Note 3 “IEEE802.3-2005 10GbE jitter mask.” Corrected figure # of section 3 and section
0.90	Sep 2020	Initial release